Intel® E7500 Scalable Performance Board Development Kit

User's Manual

August 2002

Order Number: 273693-002

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Revision History

Date	Revision	Description
August 2002	002	Added Low Voltage Intel® Xeon™ processor
March 2002	001	First release of document.

About This Manual 1

This manual tells you how to set up and use the evaluation board and other components included in your Intel® E7500 Scalable Performance Board Development Kit.

1.1 Content Overview

Chapter 1, “About This Manual” – This chapter contains a description of conventions used in this manual and instructions for obtaining literature and contacting customer support.

Chapter 2, “Getting Started” – Provides complete instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3, “Theory of Operation” – This chapter provides information on the system design.

Chapter 4, “Hardware Reference” – This chapter provides a description of jumper settings and functions, and pinout information for each connector.

Chapter 5, “Intel® Applied Computing System Firmware Library” – This chapter provides an overview of Intel ACSF Library, which is a firmware development tool kit suitable for creating custom firmware images.

Chapter 6, “BIOS Quick Reference” – This chapter describes how to configure the BIOS for your system configuration. A summary of all BIOS menu options is provided.

Chapter 7, “P64H2 Riser Card” – This chapter provides installation instructions for the P64H2 Riser Card, an optional item which may be included in this development kit.

Appendix A, “Bill of Materials” – This appendix contains the bill of materials for the evaluation board.

Appendix B, “Schematics” – This appendix contains schematics for selected connectors and subsystems for the evaluation board.

1.2 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in italics. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either upper- or lowercase.
Numbers	Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character H. A zero prefix is added to numbers that begin with A through F. (For example, FF is shown as 0FFH.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter B is added for clarity.)
Units of Measure	The following abbreviations are used to represent units of measure:

A	amps, amperes
Gbyte	gigabytes
GHz	gigahertz
Kbyte	kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
Mbyte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

Signal Names	Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (n). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CSn#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Technical Support

1.3.1 Electronic Support Systems

Intel's site on the World Wide Web (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

1.3.1.1 Online Documents

Product documentation is provided online in a variety of web-friendly formats at:
http://developer.intel.com/design/intarch

1.3.2 Additional Technical Support

If you require additional technical support, please contact your field sales representative or local distributor.

1.4 Product Literature

You can order product literature from the following Intel literature centers.

1-800-548-4725 U.S. and Canada

708-296-9333 U.S. (from overseas)

44(0)1793-431155 Europe (U.K.)

44(0)1793-421333 Germany

44(0)1793-421777 France

81(0)120-47-88-32 Japan (fax only)

1.5 Related Documents

Table 1. Related Documents

Document Title	Order Number
Low Voltage Intel® Xeon™ Processor Datasheet	273766
Low Voltage Intel® Xeon™ Processor Specification Update	273767
Low Voltage Intel® Xeon™ Processor for Embedded Applications Thermal Design Guide	273764
Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz and 2.2 GHz Datasheet	298642
Intel® Xeon™ Processor Specification Update	249678
Intel® Xeon™ Processor with 512 KB L2 Cache System Compatibility Guidelines	298645
Voltage Regulator Module (VRM) 9.0 DC-DC Converter Design Guidelines	249205
Voltage Regulator Module (VRM) 9.1 DC-DC Converter Design Guidelines	298646
Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines	298644
ITP700 Debug Port Design Guide	249679
Intel® Xeon™ Processor Thermal Design Guidelines	298348
Intel® Xeon™ Processor with 512 KB L2 Cache and Intel® E7500 Chipset Platform Design Guide	298649
Intel® E7500 Chipset Design Guide: Intel® E7500 Chipset Memory Controller Hub (MCH) Thermal and Mechanical Design Guidelines	298647
Intel® E7500 Chipset Datasheet: Intel® E7500 Chipset Memory Controller Hub (MCH)	290730
Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet	290732
Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet	290733
Intel® E7500 Chipset Memory Controller Hub (MCH) Specification Update	290731
Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Specification Update	290735
Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Specification Update	290739
Intel® 82802AB/82802AC Firmware Hub (FWH)	290658
Intel® 82802 Firmware Hub: Random Number Generator	298029
Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture	243190
Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference Manual	243191
Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide	243192
Intel® Pentium® 4 and Xeon™ Processor Optimization	248966
Intel® Applied Computing System Firmware Library User's Guide	273261
Intel® Applied Computing System Firmware Library Reference Manual	273260

Getting Started 2

This chapter identifies the Intel® E7500 Scalable Performance Board Development Kit's key components, features and specifications. It also tells you how to set up the board for operation.

2.1 Overview

The development kit contains a baseboard with two Intel® Xeon™ Processors with 512 Kbyte L2 cache, two Low Voltage Intel Xeon Processors, Intel E7500 chipset, and other system board components and peripheral connectors. Also included in the kit are a hard drive, power supply, and a board/component stand. Various software and documentation are also included in the kit.

Note: The evaluation board is shipped as an open system with a stand allowing for maximum flexibility in changing hardware configuration and peripherals in a lab environment. Since the board is not in a protective chassis, the user is required to observe extra precaution when handling and operating the system. Some assembly is required before use.

2.2 Evaluation Board Features

The evaluation board features are summarized below:

CPU

- Supports dual Intel® Xeon™ processors with 512 Kbytes of L2 cache and dual Low Voltage Intel® Xeon™ processors
- Supports 400 MHz Processor System Bus (PSB) at 3.2 Gbytes/s

Chipset

- Intel® E7500 chipset
- RGE7500PL Memory Controller Hub (MCH)
- Two Intel® 82870P2 PCI/PCI-X 64-bit Hubs 2 (P64H2)
  - — Connected to MCH via 16-bit Hub Interface 2.0 (HI 2.0) at 1.066 Gbytes/s with ECC
  - — Supports PCI-X to 133 MHz, PCI to 66 MHz
- Intel® 82801CA I/O Controller Hub 3 (ICH3-S)
  - — Connected to MCH via 8-bit Hub Interface 1.5 (HI 1.5) at 266 Mbytes/s
  - — Built-in MAC
  - — 8 Mbit 82802AC Firmware Hub (FWH)
  - — PCI 32-bit/33 MHz
  - — Two IDE controllers supporting Ultra ATA-100/66/33 IDE protocol (only one connector is available on the evaluation board)

Memory Support

- Two-channel DDR-200 memory interface at 3.2 Gbytes/s bandwidth, four slots per channel
- Registered/ECC memory only
- Two to eight DDR-1600 DIMMs
- 256 Mbytes to 16 Gbytes total memory (the system has been validated with up to 8 Gbytes of memory)

Flash System BIOS ROM

- General Software* system BIOS

Power Supply

- WTX power supply

System I/O

- On-board Intel® 82544EI Gigabit Ethernet controller
- On-board Adaptec* AIC7902 SCSI controller
- On-board video with one built-in VGA connector
- One floppy connector supporting one floppy drive
- One Ultra ATA-100/66/33 IDE connector supporting up to two IDE devices
- One built-in 16550 fast UART compatible serial port connector
- Built-in Standard/EPP/ECP parallel port connector
- Two built-in Universal Serial Bus (USB) connectors
- Built-in PS/2 keyboard and PS/2 mouse (6-pin mini-DIN) connectors

Peripheral Connectors

- One 64-bit/133 MHz PCI-X slot
- One 64-bit/100 MHz PCI-X slot
- Four 64-bit/66 MHz PCI-X slots (one contains a HI 2.0 extension)
- One 32-bit/33 MHz PCI slot (for debug and legacy support only)

2.3 Included Hardware

The following hardware is included in the development kit:

- Board/component stand and mounting hardware
- Evaluation board (baseboard) with battery
- WTX power supply
- BIOS Image from General Software* (FWH installed on board)

- Two Intel® Xeon™ Processors with 512 Kbytes L2 cache at 2.0 GHz with 400 MHz PSB (installed on board)
- Two Low Voltage Intel® Xeon™ Processors at 1.6 GHz with 400 MHz PSB
- Two fansink thermal solutions and metal attachment brackets
- Two sets of plastic processor retention mechanisms (four pieces) for the 2.0 GHz processors
- Two retention clips for the 1.6 GHz processors.
- One MCH heatsink and attachment clip
- Two 256 Mbytes DIMMs, registered with ECC
- IDE hard disk drive pre-loaded with QNX RTP*
- 80-pin IDE cable for the hard disk drive (cable will support two IDE devices
- Hardware to attach the board and the hard drive to the stand:
  - 42 screws: 6/32" (diameter) x 7/16" (length)
  - 19 female-female standoffs: 6/32" (diameter) x 5/8" (length)
  - 19 lock washers: size 6

Optionally, your kit may include a P64H2 Riser Card with installation hardware (see Chapter 7).

2.4 Software Key Features

The software in the kit was chosen to facilitate development of real-time applications based on the components used in the evaluation board. The software tools included in your kit are described in this section.

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Refer to the documentation in your development kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using tools that work with other third party products must have licensed those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

Refer to http://developer.intel.com/design/intarch/devkits for details on additional software from other third party vendors.

2.4.1 Embedded BIOS for the Intel® E7500 Scalable Performance Board Development Kit

The evaluation board is pre-installed and licensed with a copy of Embedded BIOS* from General Software, Inc. Refer to Chapter 6 for a detailed product description and instructions on using the BIOS setup.

2.4.2 Applied Computing System Firmware Library

A flash memory device containing a customized binary boot image created with the Intel Applied Computing System Firmware Library (ACSF Library) can be requested by sending an email to IACSFL@intel.com. The flash device containing the BIOS can be easily removed from its socket on the evaluation board, and replaced with the ACSF Library flash device if desired.

2.4.3 Operating Systems

2.4.3.1 Wind River Tornado* Development Platform

Wind River* is a leading provider of embedded software and services for smart devices in the Internet age. Answering the challenge of the growing needs of embedded software developers and working with Intel through the Center of Excellence program, Wind River provides advanced, optimized solutions targeted for products based on embedded Intel architecture. This means providing products that take advantage of the latest embedded features found in the processors, as well as synchronizing support for new processor architectures.

Wind River introduces Tornado* Development Platform, the optimized solution for the Intel® E7500 Scalable Performance Board Development Kit. The Tornado Development Platform includes VxWorks*, the most widely adopted real-time operating system (RTOS) in the embedded industry, as well as Tornado Tools, a comprehensive suite of core and optional cross-development tools and utilities, and a full range of communications options for the target connection to the host.

VxWorks is flexible, with more than 1800 powerful application program interfaces (APIs); scalable, from the simplest to the most complex product designs; reliable, used in mission-critical applications ranging from anti-lock braking systems to inter-planetary exploration; compatible with numerous industry standards, and available on all popular CPU platforms.

The VxWorks RTOS comprises the core capabilities of the wind microkernel along with advanced networking support, powerful file system and I/O management, and C++ and other standard run-time support. These core capabilities can be combined with add-on components available from Wind River and its more than 600 WindLink* partner companies.

Tornado* AE includes VxWorks* AE (a new protected operating system) as well as Tornado Tools 3.0, significant advances in the Tornado host development environment and host-target middleware.

Foremost among the VxWorks AE enhancements is the introduction of protection domains, an MMU-based feature of the kernel that provides for several types of protection against unintentional mistakes or errant code. A protection domain may be thought of as a container for code, data, and system objects, including tasks.

Protection domains offer the following types of protection:

- Protection of the kernel from errant application code
- Run-time isolation of applications from each other
- Inter-application linkage protection
- Text and read-only data protection
- Automatic resource reclamation

Additional VxWorks AE enhancements include:

- Fully integrated, virtual-memory-based memory management
- Physical memory management support
- An ELF section-oriented loader that supports out-of-order loading
- Improved wind kernel object management
- Stack overflow detection

Advances in the host development environment include a new multitasking debugger as the standard Tornado debugger, a new operating system object inspector (replacing the browser), enhancements throughout the IDE (and command line) to support the development of protection domains within VxWorks AE, simplification of host-target access management, and various other improvements in the host GUI.
Tornado 3 and Tornado AE offer:

- Intel Pentium® 4 processor and Hyper-Threading technology support
- 36-bit addressing
- Shared memory object
- Integrated booting strategy so users can create boot images in MP environment
- Industry accepted wind microkernel
- Protection domain management
- Resource tracking and management
- System overrun protection
- Powerful loader facilities
- Efficient deterministic task management
- Fast interrupt and exception handling
- Optimized floating-point support
- Dynamic memory management
- Networking support including large network stacks to choose from
- Fast, flexible I/O and local file system
- Advanced, integrated Tornado tools development environment

For more information, refer to the Wind River documentation included in the development kit.

2.4.3.2 QNX Realtime Platform* (RTP)

Built from over 20 years of expertise in RTOS development, the QNX Realtime OS*, a core technology of the QNX RTP, provides a powerful, massively scalable, reliable foundation for embedded systems. QNX Realtime OS offers the following features:

- **Flash File System Manager:** Features wear-leveling, on-the-fly decompression, random writes, fault recovery, and other characteristics unique to implementing a file system in flash memory.

- **CD-ROM File System Manager:** Implements the ISO-9660/Rock Ridge media standard and allows CD-ROMs and DVDs to be readily used.
- **CIFS File System Manager:** Implements the Microsoft* Common Internet File System standard and allows Windows* network file access.
- **NFS File System:** A popular network file system for enterprise-wide, heterogeneous networking, NFS lets you transparently access files on most UNIX* and Linux systems and many non-UNIX systems, including Windows.
- **Choice of TCP/IP Stacks:** QNX gives you a choice of TCP/IP stacks. Choose the Tiny TCP Manager, which provides a small implementation of TCP/IP, including ftp, ftpd, telnet, telnetd, and more. Tiny TCP also supports PPP and 802.3 networking. Or, you can use the full BSD 4.4 stack, which adds features such as routing, IP filtering, and multicasting.
- **USB Stack:** Featuring hot-swap and plug-and-play capabilities, this bus standard provides a low-cost method for adding peripheral devices to your system. The QNX RTOS implementation follows the USB 1.1 specification and supports OHCI and UHCI chips.
- **PCI Device Manager:** Provides PCI services for all managers in your system. The PCI Manager makes it possible to transparently access all PCI services.
- **Serial Manager:** Provides standard POSIX TTY device control while supporting extensions for efficient realtime protocol management.
- **PCMCIA/CardBus Server:** Ideal for small, rugged, memory-constrained devices, such as digital cameras, the PCMCIA/CardBus standard is fully supported under the QNX RTOS. The server manages host resources (memory windows, I/O ports, and IRQs) and provides utilities to start and stop processes (as cards are inserted and removed), to display server status, and to show card CIS data.

QNX Networking Infrastructure Platform

This platform is a comprehensive suite of tools and protocol stacks for OEMs building IP, optical, and storage networking equipment. It includes Qnet* micronetworking for network-distributed applications, symmetric multiprocessing (SMP), QNX High Availability Toolkit, QNX System Analysis Toolkit, plus support for a rich suite of protocol stacks (MPLS, OSPF, BGP, ATM, etc.) and tools (modeling, software measurement, etc.).

Microkernel Architecture at its Best

Tiny yet powerful, the QNX Neutrino* microkernel lies at the heart of the QNX RTOS. QNX Neutrino delivers core realtime services for embedded applications, including message passing, POSIX thread services, mutexes, condition variables, semaphores, signals, and scheduling. It can also be smoothly extended to support POSIX message queues, file systems, networking, and other OS-level capabilities with off-the-shelf, service-providing modules.

The QNX RTOS architecture offers unprecedented scalability. You can link your application code directly against the QNX Neutrino microkernel to create a single multi-threaded image for small embedded systems — as you would with a realtime executive. Or, you can run the process manager for all the advantages of a full process model and the ability to add thousands of applications — all running in MMU-protected memory. Or, applications can be run over a distributed network of SMP clusters for the ultimate in large-scale configurations. Whatever your configuration—tiny, medium, massive, or distributed— recoding is never an issue since the API remains consistent throughout.

QNX Neutrino is the world's first microkernel engineered from the ground up for the latest POSIX 1003.1 standards and drafts, including realtime and thread options. QNX Neutrino's POSIX implementation means portability of your application code and your software developers.

Programmers familiar with UNIX or Linux won't need any training to feel right at home in this POSIX environment. This built-in POSIX compatibility also comes without the penalty of extra code. Even after the process manager is added to include services like process creation, pathname-space management, and memory protection, a QNX-based system is extremely small and efficient — crucial for ROMable systems.

Conventional RTOSs use a single flat memory architecture where hard-to-detect programming errors like corrupt C pointers can cause programs to overwrite each other or the kernel. The inevitable result is system failure. A QNX-based system, however, can intelligently recover from software faults, even in drivers and other critical programs, without rebooting, because every OS component runs in its own MMU-protected address space. More importantly, because of the QNX RTOS's design, full MMU protection doesn't come at the expense of performance. With fast context-switch speeds and low latencies, QNX delivers reliable realtime performance.

Ever-evolving standards and changing customer demands can shorten the life cycle of your product. With QNX, you can dynamically upgrade and maintain your product in the field. Since all drivers, applications, and OS modules reside in their own memory-protected space, you can easily add new features or fix problems without interrupting service.

With QNX micronetworking (Qnet*) you can transparently access any resource in your system, local or remote. Qnet extends the message-based architecture of the QNX RTOS, integrating your entire network into a single, homogeneous set of resources. Even the smallest, memory-constrained device can make full use of another node's file system, servers, hardware resources, etc. Qnet provides fault-tolerant networking, load-balancing on the fly, extensible architecture, and transparent distributed processing.

Unlike some operating systems that try to squeeze monolithic designs or bulky windowing systems into embedded environments, the QNX RTOS was designed to reduce the cost and component count of your products. On custom Intel Architecture target systems, for example, you can eliminate the expense of a BIOS since QNX doesn't rely on BIOS calls. QNX was also designed to keep RAM requirements to an absolute minimum. For instance, it supports execute-in-place (XIP), which allows applications to run directly out of ROM or flash. And, since its system image is actually a simple read-only file system, QNX allows applications to start without a separate file system manager or command interpreter.

Device Drivers Made Easy Across Platforms

From the beginning, drivers for the QNX RTOS were designed to be source-code identical across CPUs and boards. In fact, the same binaries for a CPU can run on different boards — no more BSP nightmares sorting out the complexity of custom board- and processor-specific code. To reduce the time required to write your own device drivers, QNX provides a resource manager framework and C functions that handle the default behaviors common to most devices; all you need worry about are the low-level details specific to your device. And because each QNX driver runs as a standard process (rather than as part of the kernel itself), you can test changes in driver code without having to go through the time-consuming task of rebuilding the kernel. To do so, recompile and restart the driver on a running system.

A Host of Functionality and Development Options

QNX Software Systems has developed an efficient suite of embedding tools and run-time software components to provide everything from cross-platform connectivity to a full-featured embeddable windowing system.

QNX RTOS development is supported under the industry-standard GNU tool chain. Depending on your project, you can choose self-hosted QNX development or cross-development from Windows and Solaris* workstations. Whatever tools you choose, the QNX RTOS offers a number of productivity advantages for debugging and testing. Software faults can be immediately identified at the exact instruction, so problems that often take weeks or months to fix, can take only days. You can also drastically reduce testing time, since only changed modules need to be retested. Any field-tested modules (drivers, OS extensions, or applications) can be easily reused across products.

No other realtime OS scales so easily — just plug in the modules or drivers you need. Extend the functionality of your application with any of the following modules:

- **Embeddable QNX Photon* microGUI:** Offers a highly functional windowing system for resource-constrained embedded environments. Running in an extremely small memory footprint, QNX Photon delivers sophisticated functionality, including multimedia support, and connects seamlessly to the QNX RTOS's message-passing architecture.

  QNX Photon also gives you exceptional connectivity between windowing systems. With Photon's remote user interface (RUI) technology you can view and control the GUI of a QNX embedded system from a window on a Windows or UNIX desktop. RUIs are baud-rate aware and can run across a serial or network link. For embedded systems, this can give you a graphical interface into your consoleless black box.

  With the Citrix ICA* client, you can access Windows applications from your QNX-based set-top box, network computer, or any other thin client in your system.
- **Boot Modules:** Perform platform- and processor-dependent initialization for embedded systems at startup, releasing occupied memory after initialization. (Boot modules are supplied in full source for custom hardware adaptations.)
- **Process Manager:** Extends services to include support for processes (containing threads), protected memory, and pathname-space management. The pathname space can then be populated by other processes that are visible to application threads.
- **Network Manager:** Coordinates messages between local and remote nodes. The network manager module runs network drivers, protocols, and Qnet.
- **Embeddable QNX File System Manager:** Provides essential services (including hard links, long file names, etc.) of a POSIX 1003.1 file system in a low-overhead implementation.

2.5 Before You Begin

Table 2 lists additional hardware you may need for your development kit.

Table 2. Additional Hardware (Sheet 1 of 2)

VGA Monitor	You can use any standard VGA or greater resolution monitor.
Keyboard	You can use a keyboard with a PS/2 style connector or adapter.
Mouse	You can use a mouse with a PS/2 style connector or adapter.
IDE Devices	You can connect up to two IDE devices to the evaluation board. One IDE hard drive and cable are included in your kit. The cable accommodates the included hard drive and one other IDE device, such as a CD-ROM drive or another hard drive.
SCSI Devices	There are two on-board SCSI connectors, one for each channel. Each connector will support up to 15 SCSI devices. No SCSI devices or cables are included in the development kit. For additional information on SCSI, refer to Section 4.3.2.
Floppy Drive	You can connect up to two floppy drives to the connector on the evaluation board. No floppy drives or cables are included in the development kit.

Table 2. Additional Hardware (Sheet 2 of 2)

Video Adapter	You can use the on-board video adapter supplied with your kit, or you may install your own PCI video adapter. You must procure and install the correct drivers for any additional video adapters.
Network Adapter	An Intel® 82544EI Gigabit Ethernet Controller is included in the development kit. A Cat5 cable with an RJ-45 connector is required to connect this Ethernet adapter to your network. You may use a different network card other than the controller included on the board; however, you are responsible for installing the correct drivers for any additional network cards. The evaluation board supports PCI/PCI-X cards.
P64H2 Riser Card	You may have purchased a P64H2 Riser Card with your development kit. It is recommended that you install this card *after* you have initially booted and configured your system. Refer to Chapter 6 for detailed installation instructions.
Other Devices and Adapters	The evaluation board behaves much like a standard workstation or server motherboard. Many PC-compatible peripherals can be attached and configured to work with the evaluation board. For example, you may want to install a sound card or additional network adapters. You are responsible for procuring and installing any drivers required for additional devices.

2.6 Setting up the Evaluation Board

Once you have gathered the hardware described in the last section, follow the steps below to set up your development kit. This manual assumes you are familiar with basic concepts involved with installing and configuring hardware for a PC or server system. Refer to Figure 7 on page 38 for locations of connectors, jumpers, and other board components, and to Figure 8 on page 52 for locations of the peripheral connectors.

1. **Ensure a safe work environment.** Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electrostatic discharge, which may cause product failure or unpredictable operation.

Caution: Connecting the wrong cable or reversing a cable can damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.

2. **Verify kit contents.** Inspect the contents of your kit, and ensure that everything listed in Section 2.3 is included. Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.
3. **Gather tools.** You will need a Phillips-head screwdriver and a 6/32" hex wrench for installation.
4. **Check jumper settings.** Verify that the following jumpers are set correctly. For detailed descriptions of all jumpers, please refer to Section 4.5.

Table 3. Jumper Settings

Jumper	Function	Default Setting
JP1	Safe Mode	Open
JP2	Top Swap	Open
JP3	ITP Select	Short 1-2: One processor Short 2-3: Two processors
JP4	CMOS Clear	Short 1-2
JP7	No Reboot	Open
J19	Test Header	Open
J27	Write Protect	Short 1-2
JP24, JP25, JP26, JP27	PCI-X Slot 1, Bus A Mode	All open
JP28, JP29, JP30	PCI-X Slot 2, Bus B Mode	All open
JP31, JP32, JP35	SCSI PCI/PCI-X Mode	All open
JP33, JP34	PCI-X Slots A:D Mode	Both open
J36	Test Header	Open
JP38	SMBUS 0 VSBY5	Open
JP39	SMBUS 1 VCC3	Open
JP40	SMBUS 2 VCC3	Open
JP41	SMBUS 3 VCC3	Open
JP42	Loadline Select	Short 1-2: Intel® Xeon™ Processor Open: Low Voltage Intel Xeon Processor
J71	BMC Connector	Short 5-6, 7-8, 9-10, 17-18, 19-20, 29-30

5. **Verify installed hardware.** Make sure the following hardware is populated on your evaluation board:
   - — Two Intel Xeon processors or Low Voltage Intel Xeon Processor, in sockets J17 and J18
   - — BIOS FWH in socket U69
   - — Battery in battery holder BH1

Note: The above hardware should have been correctly installed at the factory. If they are not installed correctly, DO NOT power on the board. Correctly re-install the components before proceeding. If you suspect that any of the kit components has been damaged, contact your Intel field sales representative or local distributor for assistance.

6. **Install board on stand.** A board/component stand is provided in your kit. Refer to Figures 1 and 2 for placement of components on the assembled stand.

Note: If you choose not to use the stand, you must use processor retention mechanisms with Tuflok* fasteners instead of the processor retention mechanisms included in the kit. The parts (part number SP2307) can be ordered from Pencom at (650) 593-3288. (This should not be considered a recommendation or product endorsement by Intel Corporation.)

Figure 1. Assembled Board/Component Stand, Front View

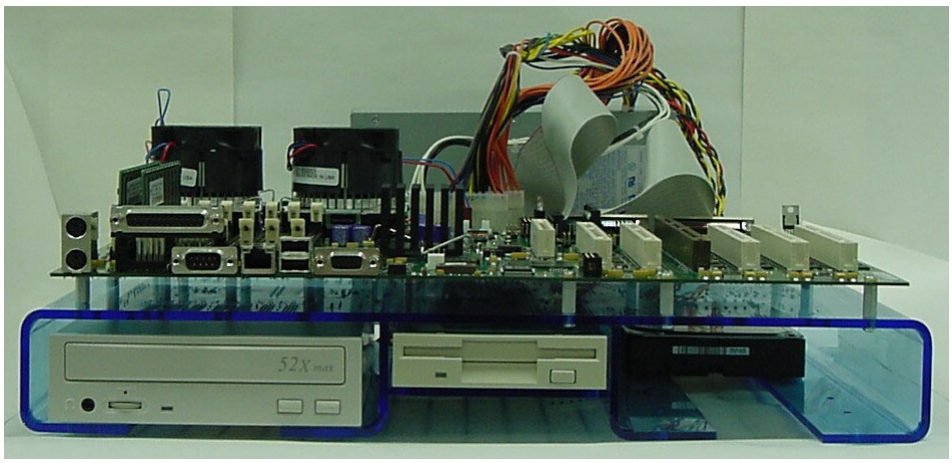
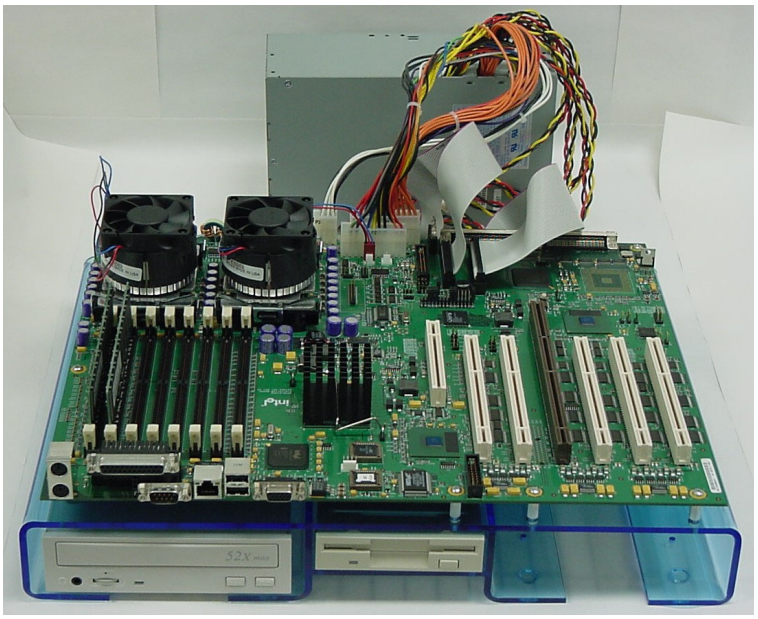


Figure 2. Assembled Board/Component Stand, Top View



To attach the board to the stand, use the following mounting hardware that is included in your kit:

- 38 screws
- 19 female-female standoffs
- 19 lock washers

The kit includes four additional screws that you will use to attach the hard drive to the stand in a later step.

See Figure 3 for a diagram of the mounting hardware. To install the board on the stand, use the following steps. To avoid damaging the board and stand, take caution not to overtighten the screws.

a. Fit a lock washer on one screw and insert it through the bottom of the top shelf of the stand.

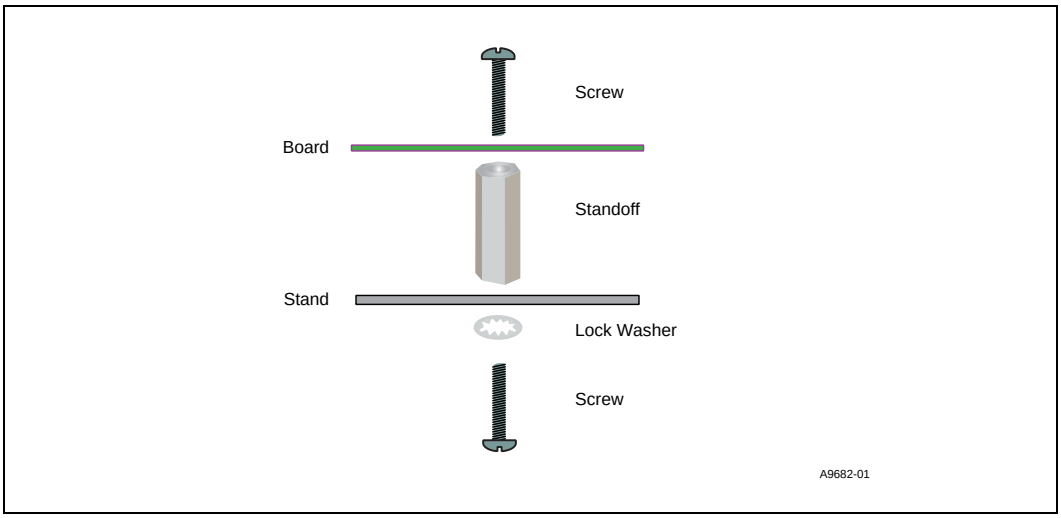
b. Using a hex wrench, screw the standoff onto the screw from the top of the shelf. Repeat for all holes in the shelf.

c. Place the board atop the standoffs, lining up the standoffs with the holes in the board. If all the holes do not line up correctly, loosen the standoffs that do not line up and re-position them.

d. Place the plastic processor retention mechanisms atop the board, lining them up above the holes astride sockets J17 and J18. Insert screws through the processor retention mechanisms into the standoffs below. Figure 4 shows one completely assembled processor assembly (rear), and one partially assembled (front).

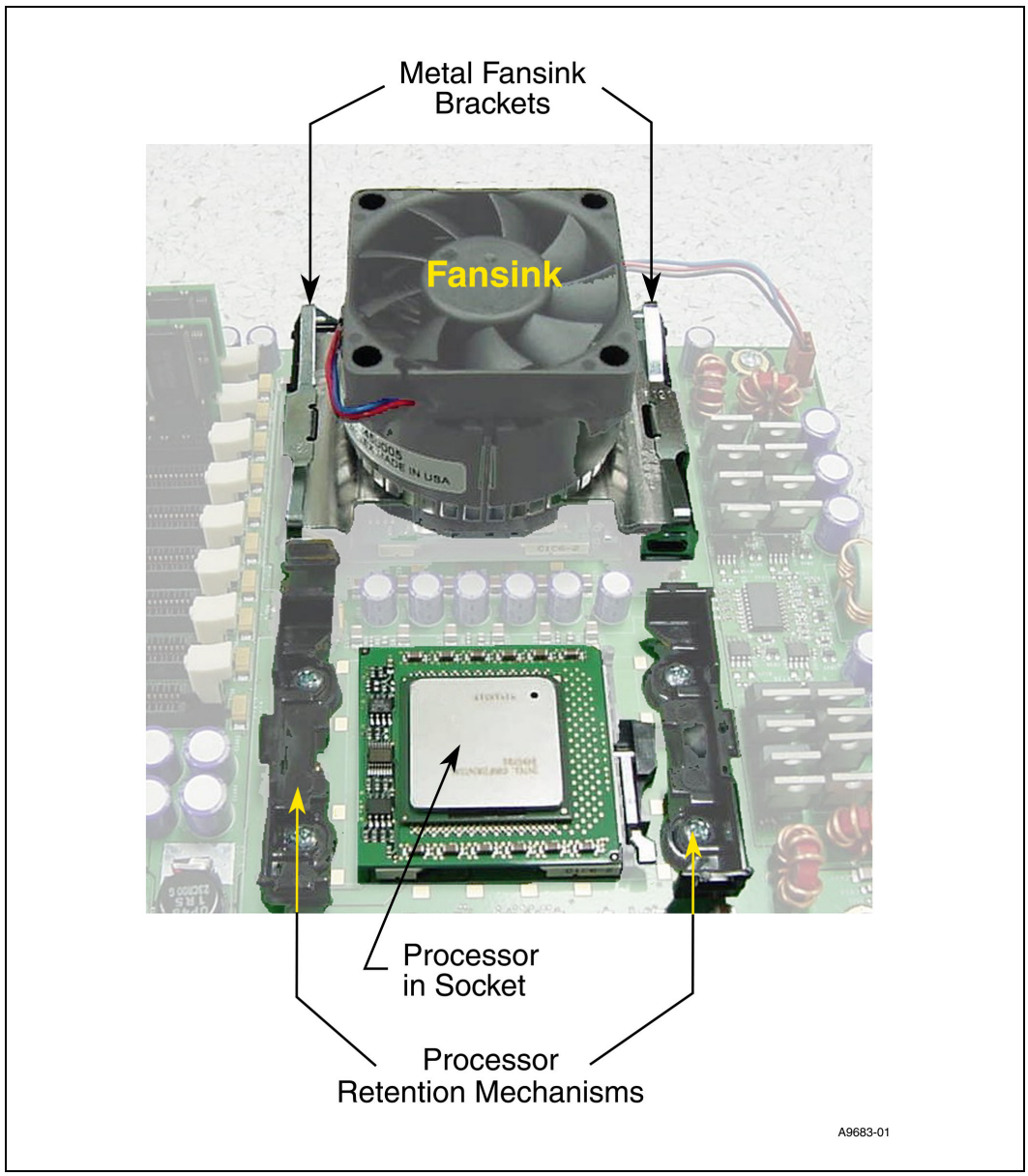
e. Insert remaining screws into the standoffs from the top of the board.

Figure 3. Mounting Hardware Installation Order



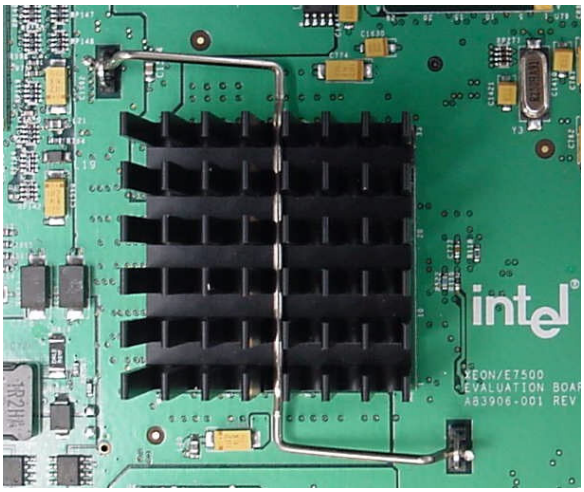
7. **Install fansinks.** You must install a fansink on each processor. Remove the green cap that is covering the thermal interface material on the bottom of the fansink. Place the fansink on top of the processor, fitting it within the plastic processor retention mechanisms. Install a metal bracket on each side of the fansink, affixing the metal rim of the fansink base to the processor retention mechanism. Repeat for the other fansink. Connect the 3-pin fansink power connectors to connectors J52 and J53 on the evaluation board. Make sure to use the proper retention clips for the Intel Xeon processors or the Low Voltage Intel Xeon processors.

Figure 4. Processor Assembly Components



8. **Install MCH heatsink.** You must install the included heatsink on the MCH (U66), using the Z-shaped metal bracket. If there is a cover on the thermal interface material on the bottom of the MCH, remove it. Place the heatsink squarely on top of the MCH. Place the center of the bracket across the center of the MCH, lining up the bracket hooks with the arch-shaped retention hooks on the evaluation board. Attach the bracket hooks to the board hooks to secure the heatsink. See Figure 5 for a picture of the installed MCH heatsink.

Figure 5. Installed MCH Heatsink



9. **Install memory.** Your kit includes two 256 Mbyte DIMMs. You must install these in memory slots J5 and J9, the two slots furthest from the MCH. To install, ensure the tabs on the slot are open, or rotated outward from the slot. Line up the DIMM above the slot (the DIMM is keyed so that it only fits in the slot in one orientation). Firmly, but carefully, insert the DIMM into the slot until the tabs close. Repeat for the other DIMM and slot.

10. **Install storage devices.** There is one IDE connector on the evaluation board, which supports two IDE devices—a master and a slave. The kit includes one IDE hard drive, preloaded with a dual-boot of QNX RTP* and Wind River VxWorks*.

    For a correct boot, ensure that the included hard drive is installed as the primary master. (Master/slave settings are determined by a jumper on each IDE device. Consult the device label/documentation to verify that the jumper is set correctly for any configuration you choose.) A CD-ROM drive or additional hard drive may be installed as a primary slave device.

    To install the included hard drive on the evaluation board:

    a. Verify that the jumper on the hard drive is set correct for “single” or “master,” depending on your configuration.

    b. Connect the short end of the IDE cable to the IDE connector J16 on the board. Ensure that the tracer on the cable is aligned with pin 1 of the connector.

    c. Connect the middle connector of the cable to the hard drive. Again, ensure that the cable tracer is aligned with pin 1 of the connector.

Note: Failure to properly align the IDE cable may damage the evaluation board and/or the hard drive.

    d. Connect a large 4-pin power connector from the power supply to the hard drive.

e. Install the CD-ROM drive (optional). A CD-ROM drive is not included in the kit and is not required, but you may find it useful in loading additional software. You must furnish your own CD-ROM drive. To install it on the evaluation board:

- Verify that the jumper on the CD-ROM drive is set for slave.
- Connect the unused end of the IDE cable you already attached to the evaluation board to the CD-ROM drive. Ensure that the cable tracer is aligned with pin 1 of the CD-ROM drive connector.
- Connect a large 4-pin power connector from the power supply to the CD-ROM drive.

f. Install the floppy drive (optional). A floppy disk drive is not included in your kit and is not required, but you may find it useful in loading additional software. You must furnish your own floppy drive(s) and cable. To install a floppy drive on the evaluation board:

- Connect the floppy cable to the floppy connector J34. Ensure that the tracer on the cable is aligned with pin 1 of the connector.
- Connect the other end of the floppy cable to the floppy drive.
- Connect a power cable to the floppy drive. Ensure that the tracer on the cable is aligned with pin 1 of the connector.

g. Install storage devices on the stand. Screws are included only for the hard drive. Place the devices on the stand as shown in Figures 1 and 2. Insert screws through the bottom of the stand into the holes on the bottom of each device.

11. **Connect the monitor.** Connect the monitor cable to the VGA port.
12. **Connect the keyboard and mouse.** Connect a PS/2 mouse and keyboard to the stacked PS/2 connector on the evaluation board. The bottom connector is for the mouse, and the top is for the keyboard. Alternatively, you can plug a USB keyboard and a USB mouse into one or both of the USB connectors on the evaluation board. Note that a legacy (PS/2) keyboard may be required for BIOS setup.
13. **Connect the network cable(s).** Connect a Cat5 cable with an RJ-45 connector to the Gigabit Ethernet port. Connect the other end of the cable to your network (e.g., hub, switch, network port).

Note: Standby voltages will be applied to the board whenever AC power is supplied. To completely power down the board, make sure to unplug the power supply from the wall. Depending on how the board was last powered off, it may turn on when the AC power is connected with no need to push the power button.

14. **Connect the power supply.** Make sure the power supply is turned off and unplugged. Connect the three WTX power supply cables to connectors J100, J101, and J102 on the evaluation board. Next, plug the power cord into the power supply and the wall.
15. **Power up the system.** Turn on the monitor, then turn on the evaluation board. The on-board power on/off button is located at S8. The on-board reset button is located at S9.

Caution: Ensure that the fansinks on the processor are operating. If they are not, turn off the power immediately and verify that the fansinks are connected to the board correctly (see Step 6). If the fansinks are still not operating, contact your Intel field sales representative or local distributor.

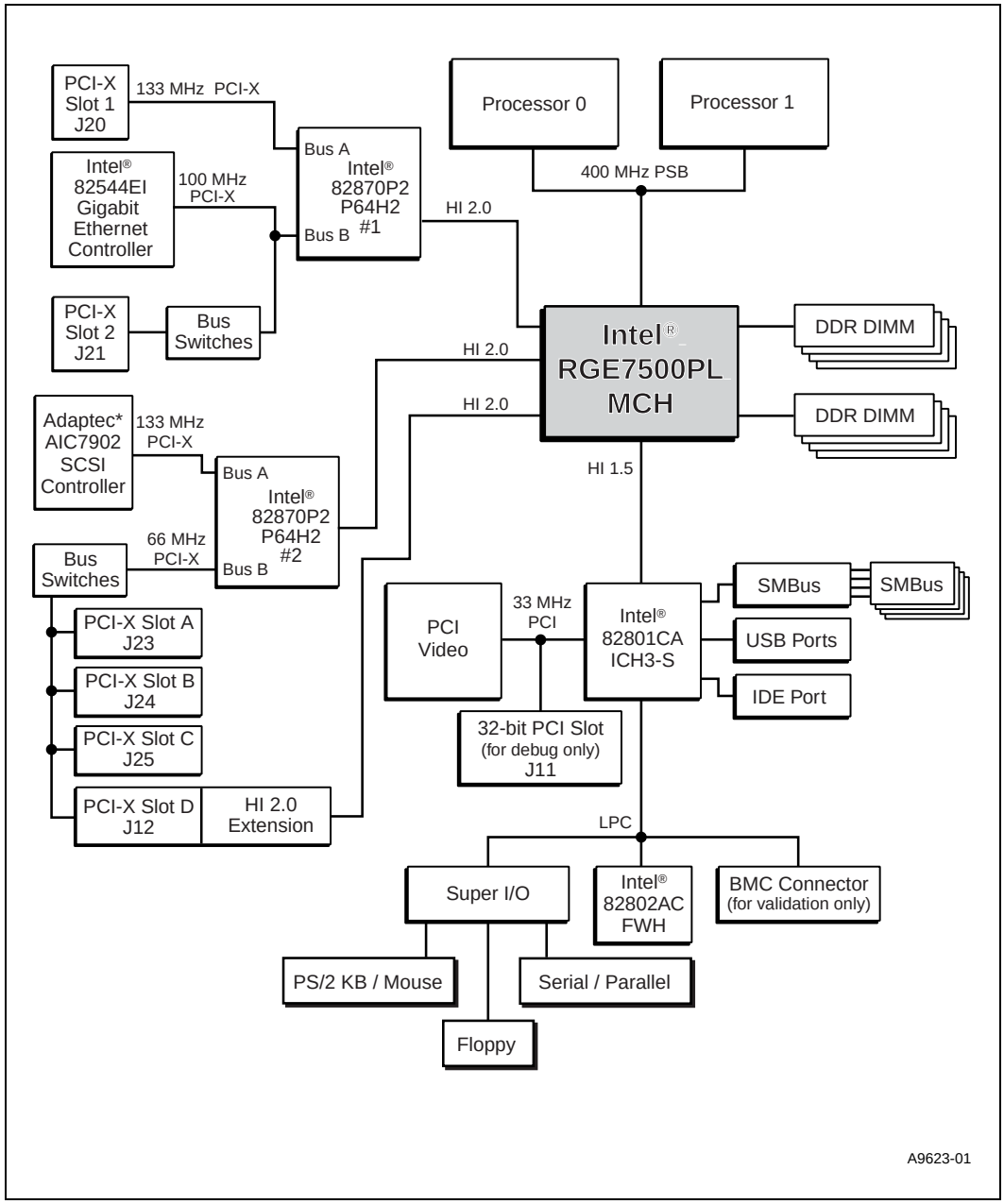
2.7 Configuring the BIOS

A General Software BIOS is pre-loaded on the evaluation board. You may need to make changes to the BIOS to enable hard disks, floppy disks and other supported features. You can use the Setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface. On first boot, you may want to use the BIOS setup program to verify the date/time and boot device. Chapter 6, “BIOS Quick Reference” contains a description of BIOS options. BIOS updates may periodically be posted to the Intel Developer web site at http://developer.intel.com/design/intarch.

Theory of Operation 3

3.1 Block Diagram

Figure 6. Block Diagram



3.2 Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance and cause reliability problems.

The development kit is shipped with fansink thermal solutions to be installed on the processors, a heatsink to be installed on the MCH and heat spreaders installed on the P64H2s. This thermal solution has been tested in an open air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

3.3 System Features

The Intel E7500 Scalable Performance Board Development Kit is designed to support the Intel® Xeon™ processor with 512 Kbyte L2 cache and the Low Voltage Intel Xeon processor. The architecture of the chipset provides the performance and feature set required for dual-processor based servers in the entry-level and mid-range, front-end and general-purpose server market segments. A new chipset component interconnect, the Hub Interface 2.0 (HI 2.0), is designed into the E7500 chipset to provide more efficient communication between chipset components for high-speed I/O. Each HI 2.0 provides up to 1.066 Gbytes/s bandwidth for high-speed I/O, which can be connected to a P64H2. The system bus, used to connect the processor with the E7500 chipset, utilizes a 400 MT/s transfer rate for data transfers, delivering 3.2 Gbytes/s. The E7500 chipset architecture supports a 144-bit wide, 200 MHz DDR memory interface also capable of transferring data at 3.2 Gbytes/s.

In addition to these performance features, E7500 chipset-based platforms also provide the RASUM (Reliability, Availability, Serviceability, Usability, Manageability) features required for entry-level and mid-range servers. These features include chipkill ECC for memory, ECC for high-performance I/O, out-of-band manageability through SMBus target interfaces on all major components, memory scrubbing and auto-initialization, processor thermal monitoring and hot-plug PCI.

3.3.1 Intel® Xeon™ Processor

The Intel E7500 chipset is coupled with these Intel Xeon processors:

- Intel Xeon processor with 512 Kbytes L2 cache with a maximum operating voltage of 1.5 V and a TDP of 58 W at 2.0 GHz
- Low Voltage Intel® Xeon™ processor with a maximum operating voltage of 1.3 V and a TDP of 30 W at 1.6 GHz

This generation of processors delivers performance levels that are significantly higher than previous generations of IA-32 processors. The Intel Xeon processor supports a 3.2 Gbytes/s data transfer rate on the processor system bus (PSB) and has 512 Kbytes of L2 cache. Uni- or dual-processor support is available.

The Intel Xeon processor and Low Voltage Intel Xeon processor are based on the Intel® NetBurst™ microarchitecture, which includes the following advanced features:

- **Hyper-Pipelined Technology:** Branch prediction/recovery pipeline is implemented in 20 stages, whereas the previous architecture was 10 stages. This enables an increase in performance, frequency and scalability.
- **400 MHz System Bus:** The highest performance Intel system bus yet allows for 3.2 Gbytes of data transfer per second over a 100 MHz core system bus clock that is quad-pumped and buffered to achieve a sustained rate of 400 MT/s.
- **Execution Trace Cache:** The L1 execution trace cache stores up to 12,000 in-order decoded micro-operations. Because the decoder has been removed from the main execution loop, instructions that are branched around are not stored, resulting in maximum utilization of this cache.
- **Rapid Execution Engine:** Two arithmetic logic units (ALUs) are clocked at twice the core frequency, allowing for basic integer operations, such as Add, Subtract, Logical AND, and Logical OR, to be executed in one-half of a clock cycle.
- **Advanced Transfer Cache:** The L2 ATC is 256 Kbytes in size and delivers a much higher throughput channel between the L2 cache and processor core.
- **Advanced Dynamic Execution:** The out-of-order execution unit is very deep, which keeps it executing instructions all the time. The execution unit can view 126 instructions in-flight and up to 48 loads and 24 stores in the pipeline. Thanks to an advanced branch prediction algorithm, the number of branch mis-predictions has been reduced 33% over the P6 generation.
- **Enhanced Floating Point and Multimedia Engine:** The floating point registers have been expanded to a full 128-bits, and an additional register has been added for data movement. This improves performance of floating point and multimedia applications.
- **Streaming SIMD (single instruction, multiple data) Extensions 2 (SSE2):** SSE2 extends the SIMD capabilities in MMX by introducing 144 new instructions, which reduces the number of instructions required to execute particular program tasks, thereby increasing performance. This accelerates a broad range of applications, including video, speech, image processing, encryption, and financial, engineering, and scientific applications.

The Intel Xeon processor and Low Voltage Intel Xeon processor also feature Hyper-Threading Technology, which provides two logical processors in one physical package. Hyper-Threading increases the performance of multi-tasking and multi-threaded applications, achieving up to a 24% increase in performance. The two logical processors have their own architectural state (data registers, segment registers, control registers, debug registers, and most model specific registers), fetch and deliver units, reorder and retire units, and xAPIC (eXtended Advanced Programmable Interrupt Controller). They share the rapid execution resources and caches, firmware, and system bus interface, and therefore, all external system resources (e.g., memory). To Hyper-Threading enabled operating systems and software, the two logical processors appear as two distinct physical processors.

The evaluation board contains two 604-pin sockets for two Intel Xeon processors or two Low Voltage Intel Xeon processors.

3.3.2 Intel® E7500 Chipset

The Intel® E7500 chipset consists of three major components: the Intel® RGE7500PL Memory Controller Hub (MCH), the 82801CA I/O Controller Hub (ICH3-S), and the Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2). Additionally, the Intel® 82802AC Firmware Hub (FWH) is connected to the ICH3-S. The chipset components communicate via hub interfaces (HIs). The MCH provides four hub interface connections: one Hub Interface 1.5 (HI 1.5) for the ICH3-S and three HI 2.0s for high-speed I/O connections to P64H2s. The hub interfaces are point-to-point and therefore only support two agents (the MCH plus one I/O device). Therefore, the MCH supports a total of three P64H2s. The evaluation board contains two P64H2s.

3.3.2.1 Intel® RGE7500PL Memory Controller Hub (MCH)

The Intel RGE7500PL MCH is a 1005-ball FC-BGA (flip-chip ball grid array) package and contains the following functionality:

System Bus Features:

- Supports dual processors at 400 MT/s
- System bus bandwidth of 3.2 Gbytes/s
- Supports 36-bit system bus addressing model
- 12 deep in-order queue, two deep defer queue

Memory Bus Features:

- 144-bit wide, DDR-200 memory interface
- Memory bandwidth of 3.2 Gbytes/s
- Supports x72, ECC, registered DDR-1600 DIMMs using 64 Mbit, 128 Mbit, 256 Mbit, and 512 Mbit DDR SDRAM
- Supports a minimum of 256 Mbytes and a maximum of 16 Gbytes of memory (evaluation board contains eight slots), populated in pairs (the system has been validated with up to 8 Gbytes memory)
- Supports up to 32 simultaneous open pages

I/O Features:

- Provides HI 1.5 connection for ICH3-S (Hub Interface A)
  - 266 Mbytes/s point-to-point connection for ICH3-S with parity protection
  - 8-bit wide, 66 MHz base clock, 4X data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing
- Provides 3 HI 2.0 connections for P64H2s (Hub Interfaces B, C, and D)
  - 1.066 Gbytes/s point-to-point connection for I/O bridges with ECC protection
  - 16-bit wide, 66 MHz base clock, 8X data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing

3.3.2.2 Intel® 82801CA I/O Controller Hub (ICH3-S)

The Intel® 82801CA ICH3-S provides the legacy I/O subsystem for E7500 chipset based platforms. Additionally, it integrates many advanced I/O functions. The ICH3-S includes the following features:

- Provides HI 1.5 Connection to MCH
  - 266 Mbytes/s point-to-point connection for ICH3-S with parity protection
  - 8-bit wide, 66 MHz base clock, 4X data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing
- Two Channel Ultra ATA-100 Bus Master IDE Controller (only one channel is utilized on the board)
- Three Universal Host Controller Interface (UHCI) USB host controllers (capabilities for six ports; only two ports are provided on the board)
- IOxAPIC
- SMBus 2.0 Controller
- LPC Interface
- AC'97 2.2 Interface (audio capabilities are not utilized on this board)
- PCI 2.2 Interface, 32-bit/33 MHz
- Integrated 10/100 Mbit Ethernet MAC (not utilized on the board)

3.3.2.3 Intel® 82870P2 PCI/PCI-X Hub 2 (P64H2)

The P64H2 provides the PCI-X, high-performance I/O capability on E7500 chipset based platforms. The P64H2 component includes:

- HI 2.0 Connection to MCH
  - 1.066 Gbytes/s point-to-point connection for I/O bridges with ECC protection
  - 16-bit wide, 66 MHz base clock, 8x data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing
- Two independent, 64-bit PCI-X Interfaces
- PCI-X 1.0 specification compliant
- PCI 2.2 specification compliant
- PCI-PCI Bridge 1.1 compliant
- One IOxAPIC per PCI-X bus segment
- PCI peer-to-peer write capability between PCI ports
- SMBus target for Out-of-Band (OOB) access to all internal PCI registers
- 16 external, 18 internal interrupts

3.3.2.4 Intel® 82802AC Firmware Hub (FWH)

The Firmware Hub (FWH) stores system BIOS and video BIOS, as well as an Intel Random Number Generator (RNG). The Intel RNG provides truly random numbers to enable stronger encryption, digital signing and security protocols. The FWH is key to enabling future security and manageability infrastructures for the PC platform. Intel 82802AC FWH features include:

- 32-Pin PLCC package
- 8 Mbit Flash memory
- Symmetrically-blocked Flash memory array (64 Kbytes memory sections)
- Pin- and register-based block locking
- Integrated hardware RNG
- Single-byte read/write
- Five General Purpose Inputs (GPIs)
- Operates with 33 MHz PCI clock and 3.3 V I/O

3.3.3 Boot ROM

The system boot ROM is installed on the Intel 82802AC FWH device, socketed at U69. The FWH is addressable on the LPC bus off the ICH3.

3.3.4 System I/O

The evaluation board contains the following I/O devices:

- On-board Gigabit Ethernet controller
- On-board SCSI controller
- Single floppy controller support
- Primary IDE interface (secondary IDE interface not implemented on board)
- One serial port
- One parallel port
- Two USB ports
- VGA port
- PS/2 keyboard and mouse ports

Please refer to Figure 7 for locations of on-board connectors, sockets, and jumpers, and refer to Figure 8 for the locations of the back panel connectors.

3.3.4.1 Intel® 82544EI Gigabit Ethernet Controller

The Intel 82544EI Gigabit Ethernet Controller with integrated PHY is Intel's single-chip Gigabit Ethernet solution. It supports PCI-X up to 133 MHz for faster network performance. It is capable of supporting 1000 Mbit/s, 100 Mbit/s, and 10 Mbit/s data rates. To use this controller on the evaluation board, utilize the built-in RJ-45 port with a Cat5 cable.

3.3.4.2 Adaptec* AIC7902 SCSI Controller

The Adaptec* AIC7902 provides Ultra320 (320 Mbytes/s) SCSI via PCI-X 133 MHz. There are two on-board SCSI connectors, each of which will support up to eight SCSI devices. For additional information on SCSI, refer to Section 4.3.2.

3.3.4.3 Floppy Disk Drive Support

One 34-pin floppy connector is provided on the evaluation board, which will support up to two floppy drives.

3.3.4.4 IDE Device Support

The evaluation board has a 40-pin connector for one of the IDE controllers present in the ICH3-S. The connector will support up to one master and one slave IDE device.

3.3.4.5 RS-232 Serial Port

The evaluation board provides one built-in serial port.

3.3.4.6 IEEE 1284 Parallel Port

One 25-pin DSUB IEEE 1284 Standard/EPP/ECP parallel port is provided on the evaluation board.

3.3.4.7 USB Ports

The evaluation board has two USB connectors.

3.3.4.8 VGA Port

The VGA port is a 15-pin DSUB female connector for output to a monitor.

3.3.4.9 Keyboard/Mouse Ports

There is one stacked PS/2 connector for a keyboard and mouse. The top connector is for the keyboard, and the bottom connector is for the mouse.

3.3.5 Expansion Slots and I/O Connectors

The evaluation board has the following expansion slots and I/O Connectors:

- One 64-bit/133 MHz PCI-X slot
- One 64-bit/100 MHz PCI-X slot
- Four 64-bit/66 MHz PCI-X slots (one contains a HI 2.0 extension, which is connected directly to the MCH via HI 2.0)
- One 32-bit/33 MHz PCI slot

3.3.5.1 PCI-X Slots

There are six PCI-X slots available on the evaluation board: one 133 MHz, one 100 MHz, and four 66 MHz.

3.3.5.2 HI 2.0 Extension

One of the 66 MHz PCI-X connectors contains a HI 2.0 extension, which is connected directly to the MCH via HI 2.0. If you purchased a P64H2 Riser Card for your development kit, you can utilize that card in this slot. See Chapter 7 for additional details on the P64H2 Riser Card.

3.3.5.3 PCI Slot

There is one 32-bit/33 MHz PCI connector on the evaluation board, for debug purposes only.

3.3.6 Post Code Debugger

An on-board Post Code Debugger is not implemented directly on the evaluation board. However, post code debugging can be accomplished through the use of a port 0080H PCI card.

3.3.7 In-Target Probe (ITP)

The evaluation board contains an in-target probe (ITP) connector for an ITP32B. You must use an ITP32B, which is specific to Intel Xeon processors and Intel® Pentium® 4 processors. Other ITPs (such as the ITP32F for Intel® Pentium® III processors) will not work.

3.3.8 Clock Generation

The clock synthesizer on the baseboard generates and distributes the clocks used by the entire system.

3.3.8.1 System Clocks

The CK408B Clock Synthesizer is the primary source of clock generation for most of the clocks on the baseboard. The following clock groups are found on the Intel E7500 Scalable Performance Board Development Kit. For more information on these clocks, see the *Intel® Xeon™ Processor with 512 KB L2 Cache and Intel® E7500 Chipset Platform Design Guide* (order number 298649).

Table 4. System Clocks

Clock Name	Clock Speed
CPU	100 MHz
PCI	33 MHz
48 MHz	48 MHz
3V66	66 MHz
REF0	4.318 MHz
USB	48 MHz
APIC	33 MHz

3.3.9 Power Supply Requirements

The Intel E7500 Scalable Performance Board uses a WTX power supply. The power supply and power cord are included in the development kit.

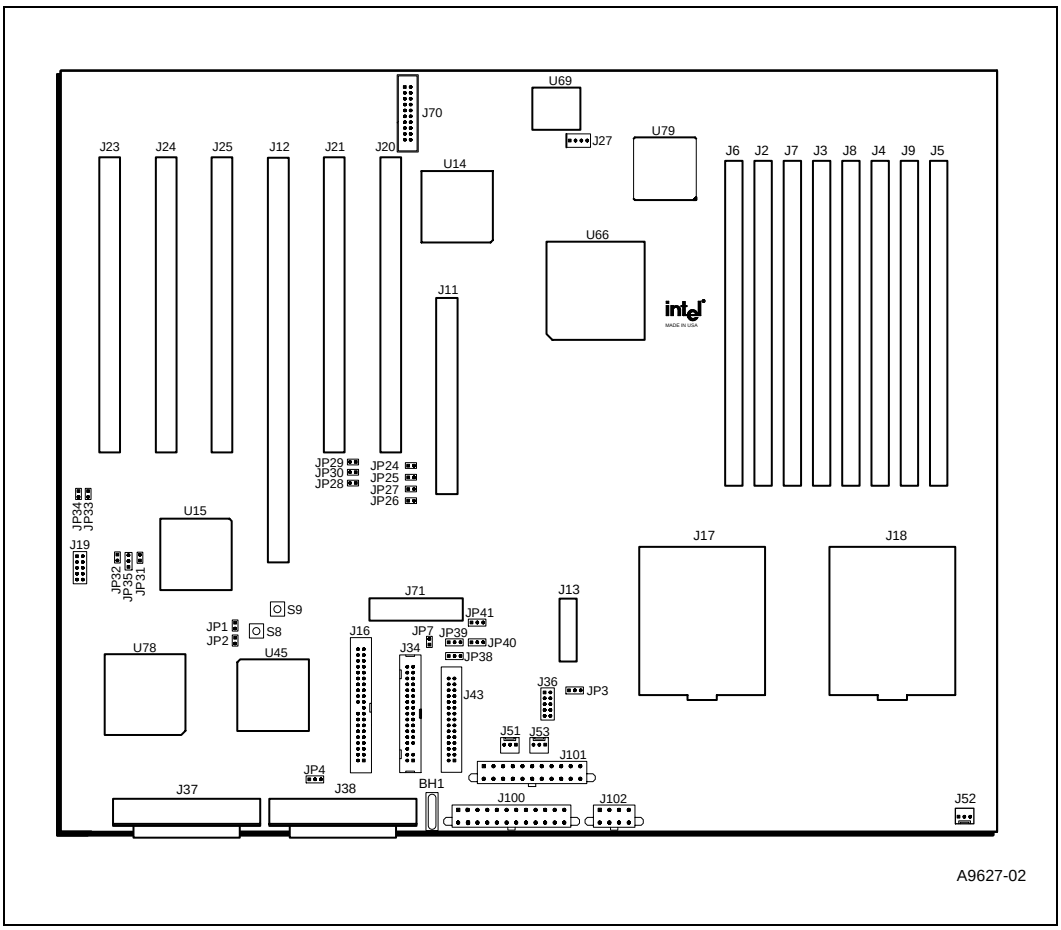
3.4 Battery Requirements

A type 2032 3V lithium coin cell battery is included on the evaluation board.

Hardware Reference 4

This section provides reference information on the hardware, including locations of evaluation board components, connector pinout information, and jumper settings.

Figure 7. Board Layout Diagram



4.1 Chipset Components

Table 5 lists the chipset and other major components on the evaluation board.

Table 5. Chipset and Major Board Components

Component Designator	Component Description
U66	Intel® RGE7500PL Memory Controller Hub (MCH)
U14, U15	Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2)
U45	Intel® 82801CA I/O Controller Hub 3 (ICH3-S)
U78	Adaptec* AIC7902 SCSI Controller
U79	Intel® 82544EI Gigabit Ethernet Controller

4.2 Expansion Slots and Sockets

Table 6 lists the expansion slots and sockets on the evaluation board.

Table 6. Expansion Slots and Sockets

Slot/Socket Reference Designator	Slot/Socket Description
J11	32/33 PCI Slot
J12	64/66 PCI-X Slot with HI 2.0 Extension (Slot D)
J20	64/133 PCI-X Slot (Slot 1, Bus A)
J21	64/100 PCI-X Slot (Slot 2, Bus B)
J23	64/66 PCI-X Slot (Slot A)
J24	64/66 PCI-X Slot (Slot B)
J25	64/66 PCI-X Slot (Slot C)
J17	Processor 1 Socket
J18	Processor 0 Socket
U69	Firmware Hub (FWH) BIOS Socket
BH1	Battery

4.2.1 32-Bit PCI Slot Connector

Table 7 shows the signals assigned to the 32-bit PCI slot connector.

4.2.2 64-bit PCI-X Connectors

Table 7. 32-bit 5V PCI Connector Pinout (J11)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	TRST#	B1	-12V	A32	AD16	B32	AD17
A2	+12V	B2	TCK	A33	3.3V	B33	C/BE2#
A3	TMS	B3	GND	A34	FRAME#	B34	GND
A4	TDI	B4	TDO	A35	GND	B35	IRDY#
A5	5V	B5	5V	A36	TRDY#	B36	3.3V
A6	INTA#	B6	5V	A37	GND	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	GND
A8	5V	B8	INTD#	A39	3.3V	B39	LOCK#
A9	CLKRUN	B9	PRSNT1#	A40	SDONE	B40	PERR#
A10	5V	B10	Reserved	A41	SBO#	B41	3.3V
A11	Reserved	B11	PRSNT2#	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	3.3V
A13	GND	B13	GND	A44	AD15	B44	C/BE1#
A14	$3.3V_{aux}$	B14	Reserved	A45	3.3V	B45	AD14
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	5V	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	PME#	B19	5V	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	3.3V	B21	AD29	A52	CBEO#	B52	AD8
A22	AD28	B22	GND	A53	3.3V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	3.3V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	3.3V	A56	GND	B56	AD3
A26	IDSEL	B26	C/BE3#	A57	AD2	B57	GND
A27	3.3V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	5V	B59	5V
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	GND	B30	AD19	A61	5V	B61	5V
A31	AD18	B31	3.3V	A62	5V	B62	5V

Table 8 shows the signals assigned to the 64-bit PCI-X connectors.

Table 8. 64-bit 3.3V PCI-X Connector Pinout (J20, J21, J23, J24, J25, J12) (Sheet 1 of 2)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	TRST#	B1	-12V	A49	AD9	B49	M66EN
A2	+12V	B2	TCK	A50	GND	B50	GND
A3	TMS	B3	GND	A51	GND	B51	GND
A4	TDI	B4	TDO	A52	CBEO#	B52	AD8
A5	5V	B5	5V	A53	3.3V	B53	AD7
A6	INTA#	B6	5V	A54	AD6	B54	3.3V
A7	INTC#	B7	INTB#	A55	AD4	B55	AD5
A8	5V	B8	INTD#	A56	GND	B56	AD3
A9	Reserved	B9	PRSNT1#	A57	AD2	B57	GND
A10	3.3V	B10	Reserved	A58	AD0	B58	AD1
A11	Reserved	B11	PRSNT2#	A59	3.3V	B59	3.3V
A12	KEY	B12	KEY	A60	REQ64#	B60	ACK64#
A13	KEY	B13	KEY	A61	5V	B61	5V
A14	$3.3V_{aux}$	B14	Reserved	A62	5V	B62	5V
A15	RST#	B15	GND		KEY		KEY
A16	3.3V	B16	CLK		KEY		KEY
A17	GNT#	B17	GND	A63	GND	B63	Reserved
A18	GND	B18	REQ#	A64	C/BE7#	B64	GND
A19	PME#	B19	3.3V	A65	C/BE5#	B65	C/BE6#
A20	AD30	B20	AD31	A66	3.3V	B66	C/BE4#
A21	3.3V	B21	AD29	A67	PAR64	B67	GND
A22	AD28	B22	GND	A68	AD62	B68	AD63
A23	AD26	B23	AD27	A69	GND	B69	AD61
A24	GND	B24	AD25	A70	AD60	B70	3.3V
A25	AD24	B25	3.3V	A71	AD58	B71	AD59
A26	IDSEL	B26	C/BE3#	A72	GND	B72	AD57
A27	3.3V	B27	AD23	A73	AD56	B73	GND
A28	AD22	B28	GND	A74	AD54	B74	AD55
A29	AD20	B29	AD21	A75	3.3V	B75	AD53
A30	GND	B30	AD19	A76	AD52	B76	GND
A31	AD18	B31	3.3V	A77	AD50	B77	AD51
A32	AD16	B32	AD17	A78	GND	B78	AD49
A33	3.3V	B33	C/BE2#	A79	AD48	B79	3.3V
A34	FRAME#	B34	GND	A80	AD46	B80	AD47
A35	GND	B35	IRDY#	A81	GND	B81	AD45
A36	TRDY#	B36	3.3V	A82	AD44	B82	GND

Table 8. 64-bit 3.3V PCI-X Connector Pinout (J20, J21, J23, J24, J25, J12) (Sheet 2 of 2)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A37	GND	B37	DEVSEL#	A83	AD42	B83	AD43
A38	STOP#	B38	PCIXCAP	A84	3.3V	B84	AD41
A39	3.3V	B39	LOCK#	A85	AD40	B85	GND
A40	SDONE	B40	PERR#	A86	AD38	B86	AD39
A41	SBO#	B41	3.3V	A87	GND	B87	AD37
A42	GND	B42	SERR#	A88	AD36	B88	3.3V
A43	PAR	B43	3.3V	A89	AD34	B89	AD35
A44	AD15	B44	C/BE1#	A90	GND	B90	AD33
A45	3.3V	B45	AD14	A91	AD32	B91	GND
A46	AD13	B46	GND	A92	Reserved	B92	Reserved
A47	AD11	B47	AD12	A93	GND	B93	Reserved
A48	GND	B48	AD10	A94	Reserved	B94	GND

4.2.3 Hub Interface 2.0 Extension

Table 9 shows the signals assigned to the Hub Interface (HI) 2.0 extension.

Table 9. HI 2.0 Extension Pinout (J12)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A95	GND	B95	GND	A113	GND	B113	GND
A96	CLK200#	B96	CLK66	A114	HI11	B114	PUSTRBF
A97	CLK200	B97	GND	A115	GND	B115	GND
A98	GND	B98	Reserved	A116	HI9	B116	HI10
A99	Reserved	B99	HI_RESET#	A117	GND	B117	GND
A100	PWR_GD	B100	HCA_PRES	A118	HI20	B118	HI8
A101	GND	B101	GND	A119	GND	B119	GND
A102	Reserved	B102	Reserved	A120	HI6	B120	HI7
A103	Reserved	B103	USE_CLK200	A121	GND	B121	GND
A104	GND	B104	GND	A122	PSTRBS	B122	HI5
A105	HI19	B105	HI18	A123	GND	B123	GND
A106	HI16	B106	HI17	A124	HI4	B124	PSTRBF
A107	GND	B107	GND	A125	GND	B125	GND
A108	HI15	B108	HI21	A126	HI2	B126	HI3
A109	GND	B109	GND	A127	GND	B127	GND
A110	HI13	B110	HI14	A128	HI0	B128	HI1
A111	GND	B111	GND	A129	GND	B129	GND
A112	PUSTRBS	B112	HI12				

4.2.4 Processor Sockets

There are two mPGA604 processor sockets on the evaluation board. For a single processor implementation, socket J18 (CPU0) must be populated, and socket J17 (CPU1) must be empty. The processor is keyed so that it fits into the socket in one particular orientation. The socket is released by lifting the cam lever.

Note: Do not force the processor into the socket, or you may damage the processor and/or socket.

The evaluation board is designed to support future processor speeds. You must use identical type and speed Intel Xeon processors or Low Voltage Xeon processors in both sockets. If you have any questions about what processors to use, contact your Intel field sales representative or local distributor.

4.2.5 Firmware Hub (FWH) BIOS Socket

The Firmware Hub (FWH), or BIOS, flash memory part fits into the 32-pin socket U69, giving you the option to remove and reprogram it without the use of soldering equipment. There is only one correct orientation for the FWH part to be placed into its socket. Line up the circular marking on the FWH part, denoting pin 1, with the circular marking on the evaluation board. Pin numbering proceeds clockwise around the chip from pin 1.

4.2.6 Battery

A type 2032 3V lithium coin cell battery is used in socket BH1 on the evaluation board. The battery holder is beveled such that the battery fits into it in one particular orientation. The battery is held in place by a metal arm. To remove the battery, bend the arm slightly toward the SCSI connector.

4.3 On-Board Connectors

Table 10 lists connector reference designators that correspond to the connectors on the board.

Table 10. On-Board Connectors

Connector Reference Designator	Connector Description
J100	WTX Main Power Connector
J101	WTX Additional Power Connector
J102	WTX $12V_{DIG}$ VRM/D2D Output Power Connector
J37	SCSI Channel A Connector
J38	SCSI Channel B Connector
J16	IDE Connector
J34	Floppy Connector
J13	ITP32B Connector
J43	Front Panel Connector
J51	Auxiliary Fan Connector
J52	CPU1 Fan Connector
J53	CPU0 Fan Connector
J71	BMC Connector
J70	Debug Connector

4.3.1 WTX Power Connectors

The following tables show the signals assigned to the three WTX power connectors.

Table 11. WTX Main Power Connector (J100)

Pin	Signal Name	Function
1	3.3V	
2	3.3V	
3	3.3V	
4	3.3V	
5	3.3V	
6	com.	Ground
7	com.	Ground
8	com.	Ground
9	com.	Ground
10	com.	Ground
11	5V	
12	5V	
13	3.3V	
14	3.3V	
15	3.3V	
16	3.3V	
17	$3.3V_{AUX}$	
18	com.	Ground
19	com.	Ground
20	com.	Ground
21	com.	Ground
22	$5V_{SB}$	
23	5V	
24	5V	

Table 12. WTX Additional Power Connector (J101)

Pin	Signal Name	Function
1	5 V_{SENSE}	5 V power supply sense line
2	3.3V_{SENSE}	3.3 V power supply sense line
3	Reserved	
4	com.	Ground
5	com.	Ground
6	12V_{IO}	
7	-12V	
8	I^2C clk	Clock signal for I^2C interface
9	FanC	Signal to control fan speed in power supply
10	PS-OK	Signal indicating all power supply outputs are within limits
11	Reserved	
12	5 $V_{SENSE\ RTN}$	Return path for 5 V power supply sense line
13	3.3$V_{SENSE\ RTN}$	Return path for 3.3 V power supply sense line
14	Reserved	
15	com.	Ground
16	12V_{IO}	
17	12V_{IO}	
18	Sleep	
19	I^2C data	Data signal for I^2C interface
20	FanM	Signal indicating fan speed/status in power supply
21	PS-on	Signal to enable/disable power supply
22	Reserved	

Table 13. WTX 12V_{DIG} VRM/D2D Output Power Connector (J102)

Pin	Signal Name	Function
1	12V_{DIG}	12 V digital
2	12V_{DIG}	12 V digital
3	12V_{DIG}	12 V digital
4	Reserved	12 V power supply digital sense line
5	com.	Ground
6	com.	Ground
7	com.	Ground
8	Reserved	Return path for 12 V power supply digital sense line

4.3.2 SCSI Connectors

Table 14 shows the signals assigned to the two SCSI connectors for the Adaptec AIC7902 SCSI Controller on the evaluation board. Connector J37 is for Channel A, and connector J38 is for channel B. Each channel will support up to 15 SCSI devices. The SCSI controller supports speeds up to Ultra-320, and you must use a cable at least as fast as the devices you wish to support on a given channel. A terminator is required on each channel. Each device on a channel must have a unique SCSI ID (0-15).

Table 14. 68-pin Single-Ended/Low Voltage Differential SCSI Connector Pinout (J37, J38)

Pin	Signal Name (SE/LVD)	Pin	Signal Name (SE/LVD)
1	SR/+DB12	35	-DB12/-DB12
2	SR/+DB13	36	-DB13/-DB13
3	SR/+DB14	37	-DB14/-DB14
4	SR/+DB15	38	-DB15/-DB15
5	SR/+DBP1	39	-DBP1/-DBP1
6	SR/+DB0	40	-DB0/-DB0
7	SR/+DB1	41	-DB1/-DB1
8	SR/+DB2	42	-DB2/-DB2
9	SR/+DB3	43	-DB3/-DB3
10	SR/+DB4	44	-DB4/-DB4
11	SR/+DB5	45	-DB5/-DB5
12	SR/+DB6	46	-DB6/-DB6
13	SR/+DB7	47	-DB6/-DB6
14	SR/+P_CRCA	48	-DBP/-P_CRCA
15	GND/GND	49	GND/GND
16	DIFFSENSE	50	GND/GND
17	TPWR/TPWR	51	TPWR/TPWR
18	TPWR/TPWR	52	TPWR/TPWR
19	Reserved/Reserved	53	Reserved/Reserved
20	GND/GND	54	GND/GND
21	SR/+ATN	55	-ATN/-ATN
22	GND/GND	56	GND/GND
23	SR/+BSY	57	-BSY/BSY
24	SR/+ACK	58	-ACK/-ACK
25	SR/+RST	59	-RST/-RST
26	SR/+MSG	60	-MSG/-MSG
27	SR/+SEL	61	-SEL/-SEL
28	SR/+C/D	62	-C/D/-C/D
29	SR/+REQ	63	-REQ/-REQ
30	SR/+I/O	64	-I/O/-I/O
31	SR/+DB8	65	-DB8/-DB8
32	SR/+DB9	66	-DB9/-DB9
33	SR/+DB10	67	-DB10/-DB10
34	SR/+DB11	68	-DB11/-DB11

4.3.3 IDE Connector

Table 15 shows the signals assigned to the IDE connector.

Table 15. IDE Connector Pinout (J16)

Pin	Signal	Pin	Signal
1	Reset IDE	21	DRQ3
2	Ground	22	Ground
3	Host Data 7	23	I/O Write#
4	Host Data 8	24	Ground
5	Host Data 6	25	I/O Read#
6	Host Data 9	26	Ground
7	Host Data 5	27	IOCHRDY
8	Host Data 10	28	Ground
9	Host Data 4	29	DACK3#
10	Host Data 11	30	Ground
11	Host Data 3	31	IRQ14
12	Host Data 12	32	Reserved
13	Host Data 2	33	Addr1
14	Host Data 13	34	Primary IDE Cable Detect
15	Host Data 1	35	Addr 0
16	Host Data 14	36	Addr 2
17	Host Data 0	37	Chip Select 0#
18	Host Data 15	38	Chip Select 1#
19	Reserved	39	Activity
20	Key	40	Ground

4.3.4 Floppy Drive Connector

Table 16 shows the signals assigned to the floppy drive connector.

Table 16. Floppy Drive Connector Pinout (J34) (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	Ground	2	Drive Enable 0
3	Ground	4	Reserved
5	Key	6	Drive Enable 1
7	Ground	8	Index
9	Ground	10	Motor Enable A#
11	Ground	12	Reserved
13	Ground	14	Drive Select A#

Table 16. Floppy Drive Connector Pinout (J34) (Sheet 2 of 2)

Pin	Signal	Pin	Signal
15	Ground	16	Reserved
17	Ground	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	Ground	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

4.3.5 ITP32B Connector

See Section 3.3.7 and ITP documentation for information on the In-Target Probe (ITP).

4.3.6 Front Panel Connector

The development kit is not shipped with a chassis, so the front panel connector is unused by default. However, if you wish to place your evaluation board in a chassis, refer to the following table for the pinout of the front panel connector.

Table 17. Front Panel Connector (J43)

Pin	Signal	Pin	Signal
1	Reserved	16	Power button
2	Ground	17	Reserved
3	Chassis Intruder	18	Ground
4	Hard drive activity LED	19	Fan Tachometer 0
5	3.3V	20	Fan Tachometer 4
6	Reserved	21	Fan Tachometer 1
7	Reserved	22	Fan Tachometer 5
8	Power LED	23	Fan Tachometer 2
9	Reserved	24	Fan Tachometer 6
10	Ground	25	Fan Tachometer 3
11	Reserved	26	Fan Tachometer 7
12	Reserved	27	Reserved
13	Reserved	28	Ground
14	Reset button	29	I^2C bus 0 clock
15	5V standby voltage	30	I^2C bus 0 data

4.3.7 Fan Connectors

There are three 12V fan connectors on the evaluation board. Use connectors J53 and J52 for the CPU0 and CPU1 fansinks, respectively. If you install another 12V fan or fansink on your evaluation board, you may use the auxiliary fan connector J51.

4.3.8 BMC Connector

The evaluation board contains a baseboard management controller (BMC) connector used in validation. The following pins must be shorted with jumpers for proper system operation: 5-6, 7-8, 9-10, 17-18, 19-20, 29-30.

4.4 DDR SDRAM Slots

The evaluation board contains eight DIMM slots for DDR SDRAM.

Table 18. DDR SDRAM Slots

DDR SDRAM Slot Designator	DDR SDRAM Slot Description
J6	DIMM 1, Channel B
J2	DIMM 1, Channel A
J7	DIMM 2, Channel B
J3	DIMM 2, Channel A
J8	DIMM 3, Channel B
J4	DIMM 3, Channel A
J9	DIMM 4, Channel B
J5	DIMM 4, Channel A

The eight DIMM slots run parallel on two channels. You must populate channels A and B together with identical DIMMs starting at the outermost DIMM slots, those furthest from the MCH (U66). For example, you must populate slots J5 and J9 (DIMM 4 on Channels A and B) first, and they must contain memory of exactly the same type and size. You would next populate slots J4 and J8. Pairs of DIMM slots may differ in size. You may use DIMMs of 128 Mbytes through 2 Gbytes. All DIMMs must be ECC registered memory. Do not mix component types—you must use all x4 or all x8 DIMMs on the evaluation board.

4.5 Jumpers

The evaluation board has a number of jumpers that control various functions of the system. Refer to Table 19 for descriptions of the jumpers and their settings.

Table 19. Jumpers (Sheet 1 of 2)

Reference Designator	Functional Description	Settings
NOTE: For groups of jumpers with multiple options, the default setting is noted with italics.		
JP1	Safe Mode	**Open (default):** Normal mode. **Shorted:** Forces processors to operate at lowest internal frequency. For debug only. Refer to the Intel® 82801CA I/O Controller Hub 3 (ICH-S) Datasheet (order number 290733) for more information.
JP2	Top Swap	**Open (default):** Normal mode. **Shorted:** The ICH3 supports a "Top-Block Swap" mode, wherein the ICH3 swaps the top block (the boot block) in the FWH with another location. This allows for safe update of the boot block. Refer to the Intel® 82801CA I/O Controller Hub 3 (ICH-S) Datasheet (order number 290733) for more information.
JP3	ITP Select	**Short 1-2:** One processor **Short 2-3:** Two processors Use the appropriate setting for the number of processors populated on the evaluation board.
JP4	CMOS Clear	**Short 1-2 (default):** Normal mode. **Short 2-3:** To clear all CMOS settings, power down, short pins 2-3 for several minutes, move the jumper back to 1-2, and boot the system.
JP7	No Reboot	**Open (default):** Normal TCO timer reboot functionality: reboot after second timeout. **Short:** Disables TCO timer system reboot feature.
J19	Test Header	Used during manufacturing only.
J27	FWH Write Protect	**Open:** All blocks write enabled. **Short 1-2 (default):** Top block write protected. **Short 3-4:** Blocks 2-8 write protected. **Short 1-2 and 3-4:** All blocks write protected.
JP24, JP25, JP26, JP27	PCI-X Slot 1, Bus A Mode	**JP24** / **JP25** / **JP26** / **JP27** / **Mode** / **MHz** *Open* / *Open* / *Open* / *Open* / *PCI-X* / *133* Short / Open / Open / Open / PCI-X / 100 Short / Open / Short / Open / PCI-X / 66 Short / Short / Short / Open / PCI / 66 Short / Short / Short / Short / PCI / 33
JP28, JP29, JP30	PCI-X Slot 2, Bus B Mode	**JP28** / **JP29** / **JP30** / **Mode** / **MHz** *Open* / *Open* / *Open* / *PCI-X* / *100* Open / Open / Short / PCI-X / 66 Open / Short / Short / PCI / 66 Short / Short / Short / PCI / 33

Table 19. Jumpers (Sheet 2 of 2)

Reference Designator	Functional Description	Settings				
JP31, JP32, JP35	SCSI PCI/PCI-X Mode	**JP31**	**JP32**	**JP35**	**Mode**	**MHz**
		Open	*Open*	*Open*	*PCI-X*	*133*
		Open	Short	Open	PCI-X	100
		Open	Short	1-2	PCI-X	66
		Open	Short	2-3	PCI	66
		Short	Short	2-3	PCI	33
JP33, JP34	PCI-X Slots A:D Mode	**JP33**	**JP34**	**Mode**	**MHz**	
		Open	*Open*	*PCI-X*	*66*	
		Open	Short	PCI	66	
		Short	Short	PCI	33	
J36	Test Header	Used for validation purposes only.				
JP38	SMBUS 0 VSBY5	These headers are used to connect to the SMBUS. See Section 4.5.1 for pinouts.				
JP39	SMBUS 1 VCC3					
JP40	SMBUS 2 VCC3					
JP41	SMBUS 3 VCC3					
JP42	Loadline Select	**Short 1-2:** Intel Xeon processor **Open:** Low Voltage Xeon processor				

4.5.1 SMBUS Headers

The SMBUS headers are used to connect the SMBUSes. Refer to Table 20 through Table 23 for pinout information.

Table 20. SMBUS 0 VSBY5 (JP38)

Pin	Pin Description
1	I^2C bus 0 data
2	Ground
3	I^2C bus 0 clock

Table 21. SMBUS 1 VCC3 (JP39)

Pin	Pin Description
1	I^2C bus 1 data
2	Ground
3	I^2C bus 1 clock

Table 22. SMBUS 2 VCC3 (JP40)

Pin	Pin Description
1	I^2C bus 2 data
2	Ground
3	I^2C bus 2 clock

Table 23. SMBUS 3 VCC3 (JP41)

Pin	Pin Description
1	I^2C bus 3 data
2	Ground
3	I^2C bus 3 clock

4.6 Buttons

The evaluation board has power and reset buttons. Refer to Table 24 for descriptions of the buttons.

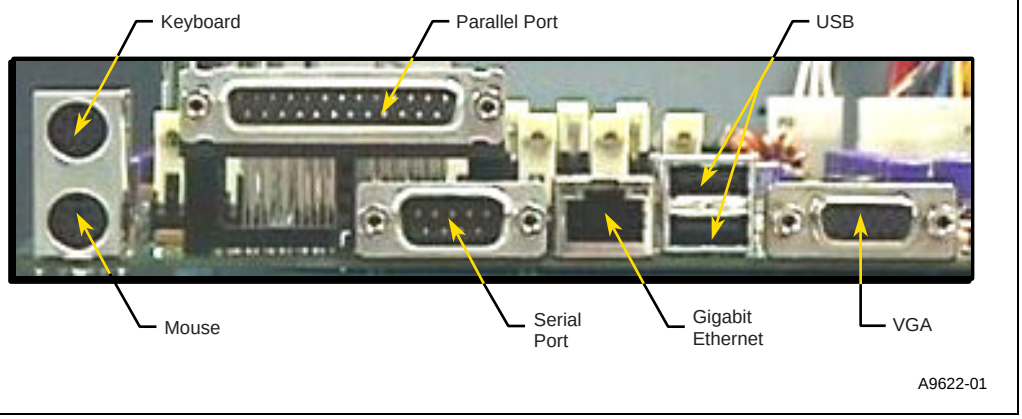
Table 24. Buttons

Switch Reference Designator	Switch Description
S8	Power Button
S9	Reset Button

4.7 Peripheral Connectors

The evaluation board contains a number of connectors for external system devices and peripherals.

Figure 8. Peripheral Connectors



4.7.1 Dual Stacked USB Connector

Table 25 shows the signals assigned to the dual stacked USB connector.

Table 25. USB Connector Pinout

Pin	Signal
1,5	Power (fused)
2,6	USBP0# [USBP1#]
3,7	USBP0 [USBP1]
4,8	Ground

4.7.2 PS/2-Style Mouse and Keyboard Connectors

Table 26 shows the signals assigned to the PS/2-style keyboard and mouse connectors. The keyboard port is on the top, and the mouse port is on the bottom.

Table 26. PS/2-Style Mouse and Keyboard Pinout

Pin	Signal
1, 7	Data
2,8	Reserved
3,9	Ground
4,10	+5 V (fused)
5,11	Clock
6,12	Reserved

4.7.3 VGA Port

Table 27 shows the signals assigned to the VGA port.

Table 27. VGA Port Signals (Sheet 1 of 2)

Pin	Signal
1	Red
2	Green
3	Blue
4	Ground
5	Ground
6	Analog Ground
7	Analog Ground
8	Analog Ground
9	Ground
10	Ground
11	Reserved

Table 27. VGA Port Signals (Sheet 2 of 2)

Pin	Signal
12	DDC Data
13	Horizontal Sync
14	Vertical Sync
15	DDC Clock

4.7.4 Parallel Port

Table 28 shows the signals assigned to the parallel port connector.

Table 28. Parallel Port Connector Pinout

Pin	Signal	Pin	Signal
1	Strobe#	14	Auto Feed#
2	Data Bit 0	15	Fault#
3	Data Bit 1	16	INIT#
4	Data Bit 2	17	SLC IN#
5	Data Bit 3	18	Ground
6	Data Bit 4	19	Ground
7	Data Bit 5	20	Ground
8	Data Bit 6	21	Ground
9	Data Bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Paper end	25	Ground
13	SLCT		

4.7.5 Serial Ports

Table 29 shows the signals assigned to the serial port connector.

Table 29. Serial Port Connector Pinout

Pin	Signal
1	DCD
2	Serial In (SIN)
3	Serial Out (SOUT)
4	DTR
5	Ground
6	DSR
7	RTS
8	CTS
9	RI

4.7.6 Gigabit Ethernet RJ-45 Connector

Table 30 shows the signals assigned to the gigabit Ethernet RJ-45 connector. A Cat5 cable with an RJ-45 connector is required to connect this Ethernet adapter to your network.

Table 30. Gigabit Ethernet RJ-45 Connector Pinout

Pin	Signal
1	Data 0 +
2	Data 0 -
3	Data 1 +
4	Data 1 -
5	Data 2 +
6	Data 2 -
7	Data 3 +
8	Data 3 -

Intel® Applied Computing System Firmware Library 5

A flash memory device containing a customized binary boot image created with the Intel® Applied Computing System Firmware Library (ACSF Library) can be requested by sending an email to IACSFL@intel.com. The flash device containing the BIOS can be easily removed from its socket on the evaluation board, and replaced with the ACSF Library flash device if desired.

5.1 Overview

The ACSF Library is a firmware development tool kit suitable for creating custom firmware images. The ACSF Library distribution in the development kit includes the following:

- Customizable sample source files for controlling the sequence of desired board initialization steps
- Libraries for linking available functionality in to the custom binary image
- Sample makefiles and linker scripts for customizing the binary image
- Standard product documentation
- A flash memory device containing a sample binary image created with ACSF Library

The software components and documentation included in the ACSF Library distribution can be downloaded from http://developer.intel.com/platforms/applied/software/firmware/acsfl/.

ACSF Library is appropriate for customers who do not need a full-featured BIOS. Its primary purpose is to help customers who are developing embedded systems improve their time to market by providing a highly modular, flexible firmware development kit.

The following is a brief list of characteristics of the ACSF Library:

- Libraries were built using the GNU tool chain. Users can utilize GNU tools to build their custom binary image.
- The vast majority of the code in the libraries was developed using 32 bit GNU C. User code may also be written in 32 bit GNU C.
- ACSF Library switches the processor into protected mode immediately after system reset, and only switches back to real mode to execute legacy code like option ROMs, or if specifically directed by the user. The protected mode environment gives the user much greater flexibility than traditional real mode firmware.
- Boot times using images created with ACSF Library are usually faster than boot times using BIOS.
- A custom binary image built using ACSF Library is usually smaller than a BIOS image.
- ACSF Library is completely modular. If a user does not want certain functionality, they simply do not link it into the custom binary image.

- ACSF Library supports a specific list of validated peripherals and operating system boot loaders. It will not generically support all PCI devices, for example. See the readme file included in the kit's ACSF Library distribution for details pertaining to the specific devices and operating systems that ACSF Library will support. ACSF Library users who need to use devices other than those in the supported list may need to develop appropriate device initialization code.

5.2 Default Distribution Feature Overview

More details on supported functionality are included in the ACSF Library documentation in the kit's ACSF Library distribution. The following list should give readers an overview of the type of functionality provided:

- Basic memory subsystem initialization for all memory configurations supported by the development kit
- Basic processor initialization including switching to protected mode, processor cache initialization and control, cache rule of conduct control, and processor microcode update functionality
- Basic chipset initialization necessary to prepare for a transition to an operating system boot loader
- PCI enumeration and resource allocation
- Hard disk drive boot of the operating systems included in the development kit
- Video subsystem initialization for a PCI VGA device
- A GNU debugger (GDB) stub which enables remote debugging of the evaluation board using a serial interface
- A rudimentary boot management interface which allows users to choose whether to boot from the hard drive, boot using PXE, or instantiate the GDB stub
- Basic initialization of most components on the Super I/O chip

The following is a list of examples of functionality that ACSF Library does not provide. The list is not comprehensive. Users who need any of the features listed below, or other functionality not provided by ACSF Library must either develop the functionality, or use a full featured BIOS:

- AGP initialization
- System management initialization and interrupt (SMI) handling
- Power management (ACPI) subsystem initialization and functionality

5.3 Documentation Included in the Distribution

The following is a list of ACSF Library documents included with the kit's ACSF Library distribution:

- User's Guide
- Reference Manual
- License Agreement
- Readme.txt

5.4 License and Support

Refer to the license agreement included with the kit's ACSF Library distribution.

Contact your Intel Field Sales Representative for additional information pertaining to future ACSF Library releases, or to provide input on the desired feature set for future ACSF Library releases.

BIOS Quick Reference 6

The evaluation board is licensed with a copy of Embedded BIOS and Embedded DOS software from General Software, Inc.[1] This software is provided for demonstration purposes only and must be licensed directly from General Software, Inc. for integration with new designs. General Software may be reached at (800) 850-5755, on the Web at http://gensw.com, or by e-mail at sales@gensw.com.

6.1 Introducing Embedded BIOS

General Software's Embedded BIOS brand BIOS (Basic Input/Output System) pre-boot firmware is the industry's standard product used by most designers of embedded x86 computer equipment in the world today. Its superior combination of configurability and functionality enables it to satisfy the most demanding ROM BIOS needs for embedded designers. Its modular architecture and high degree of configurability make it the most flexible BIOS in the world.

Although Embedded BIOS can be made to behave like a PC BIOS, it has a fundamentally different role. The goal of a PC BIOS is to provide the same standard user experience for all the systems it runs on. This allows a wide range of users to intuitively use any computer, regardless of brand, for example. The goal of Embedded BIOS is different—it allows the embedded equipment manufacturer to differentiate its product from competing products in a way that is quick and cost effective—allowing the manufacturer to pass savings on to the end user.

This operating guide describes all of the possible user features of Embedded BIOS. Most of these features are included in the demonstration BIOS on this platform, but not all can be included, either due to space limitations or because features have conflicting requirements. Some features require hardware support that isn't present in all designs. A list of included and available features in the BIOS browser is included in your demonstration BIOS. Instructions for accessing the BIOS browser are found later in this guide.

Once you move from the demonstration BIOS to your own custom adaptation, you may choose to incorporate some or all of the applicable features, modifying them as necessary to fit your application. Therefore, some of the features discussed in this operating guide may not apply to your system's demonstration BIOS.

6.1.1 Overview of Embedded BIOS Features

Dedicated to the embedded 80x86-based market, Embedded BIOS offers special-purpose features not provided by typical PC BIOS implementations.

Embedded BIOS's CPU-specific personality modules allow support of high-integration processors that have on-board timers, DMA controllers, serial ports, watchdog timers, power management, and other features.

1. General Software™, the GS Logo, Embedded BIOS™, BIOStart™, CE-Ready™, and Embedded DOS™ are trademarks or registered trademarks of General Software, Inc.

With chipset support, virtually any add-on chipset, or CPU with on-board chipset can be supported by Embedded BIOS. Traditionally, chipsets provide DRAM memory management, bus control, and address space management. The Embedded BIOS architecture provides for chipset personality modules that can be selected for a project.

Embedded BIOS's board-level support provides for the OEM to control the BIOS's access to chipset and CPU modules in major or subtle ways. Essentially a routing module, the board module contains routines, which call associated routines in the chipset and CPU personality modules. The board module routines can be modified as needed to replace the calls to the underlying CPU and chipset modules with custom code, as needed for hardware designs that work differently than standard reference designs supported by General Software.

Embedded BIOS is implemented in hand-optimized 80x86 assembly language, with special code paths for many generations of processors. The code paths have been hand-tuned to minimize the interrupt latency commonly found in desktop BIOS implementations, and many of the hot paths of the BIOS have been straight-line optimized for the common case.

ROM disk software is integrated directly with the system BIOS itself, eliminating the need to populate the ROM scan area with ROM BIOS extensions to simulate one or more floppy or hard disks in ROM. Instead, with the ROM disk configuration feature enabled, an image of a floppy or hard disk can be stored in ROM anywhere in the address space of the evaluation board and treated as a solid-state drive. If the ROM disk feature is enabled, the ROM disk can be selectively turned on or off in the setup screen.

RAM disk software is also integrated directly into the system BIOS to support PCMCIA SRAM cards and other RAM areas as floppy or hard disk emulators. SETUP even has a formatting screen for the RAM disk.

The system BIOS supports a Resident Flash Disk (RFD) that provides read/write access to sectored Flash devices as though they were a floppy or hard disk of up to 32 Mbytes. The inclusion of this software makes it easy to support Flash in embedded and hand-held consumer electronics. Multiple RFDs can be supported in the same evaluation board.

The integrated BIOS debugger gives the engineer bringing up new hardware the capability of debugging the hardware with powerful tools like a disassembler, breakpoints, CMOS editing, A20-line gating commands, cache control commands, PCI bus management commands, and Super I/O controls. The debugger is very useful for debugging chipset modules, CPU class modules, and initialization of user ROM extensions and hardware. Like the setup screen, the integrated BIOS debugger can run directly on a PC keyboard and video screen, or it can be redirected over an RS-232 serial link.

Embedded systems deployed into more inaccessible areas need watchdog timer support, so that they can automatically restart in the event that application or system software fails. Embedded BIOS provides watchdog timer control functions to allow operating systems and application programs to use watchdog timer hardware found in chipsets and certain CPU classes.

Keyboard and video output may be selectively redirected over RS-232 serial links for different system components. For example, standard console I/O, such as that used by DOS and DOS applications, can be redirected over any COM port, including those built-into high-integration CPUs. Debugger I/O and Setup screen I/O can also be redirected over the same or different RS-232 serial links.

A special manufacturing mode feature provides the necessary provisions for programming electronics products through a high-speed serial link, and then testing and repairing the same items in the field at service centers. The OEM can write custom software that uses Embedded BIOS manufacturing mode functions to perform virtually any maintenance or programming task on the evaluation board under host control.

A special System Management Mode (SMM) operating environment (Firmbase) is enabled by Embedded BIOS. This operating environment loads and executes 32-bit portable executable firmware applications from the ROM, running them inside the protective envelope of SMM. Embedded BIOS uses Firmbase and its associated 32-bit USB stack to support legacy USB and other applications. ODM/OEM-written applications, supporting high availability and other initiatives, can be written using the General Software Firmbase SDK. For more information about Firmbase and how to develop firmware applications that run inside SMM, contact General Software.

Embedded BIOS provides an integrated HTML browser, incorporating a text-based rendering of HTML pages stored as ROM files in the BIOS ROM on the platform. This browser is used on this board to provide on-line information about the platform that will not get separated from the platform, like paper documentation could. As well, the browser can be used in ODM/OEM designs to quickly develop an HTML-based user interface for an Embedded application. The browser supports text mode video displays, as well as character-based console redirection over RS232 links. For more information about the integrated browser in Embedded BIOS, contact General Software.

The Embedded BIOS registration screen feature allows you to register to receive support directly from General Software. The platform is fully functional, whether it is registered or not. If it is not registered, it does include a 15 second boot-time delay during POST. This delay is eliminated when the system is registered. The system can be registered or unregistered at any time, using General Software's on-line web site at http://www.gensw.com/register. Please see Section 6.7 for details on how to register your platform to receive technical support and reduce boot time delay.

6.1.2 PC BIOS Features

Embedded BIOS provides a comprehensive Power-On Self-Test (POST) algorithm that is automatically configured for the peripherals and capabilities selected by the adaptation engineer. During POST, hardware is initialized and tested, including the CPU, RAM, and peripherals. POST provides beep code diagnostics for errors when a display is not available, as well as error message diagnostics on the display when available. POST can also be configured to output status report codes to a manufacturing port (typically, port 80h) so that automated quality assurance (QA) equipment can determine the status of a system during POST. A special set of ASCII POST status codes are also available through a serial port, for flexibility in the debugging process when new hardware is being brought up. Either POST code system, or both, can be used during debugging.

The Embedded BIOS Setup screen system is configurable at the source level by the adaptation engineer to contain any combination of subscreens, including Basic CMOS Configuration, Custom Configuration, Shadow Configuration, Diagnostics screens, Manufacturing Mode, Debugger access, and formatting of drive emulators such as RAM and RFD drives. Setup screens can also be customized at the source level (in the board personality module) to contain custom fields as required by the application.

The BIOS browser is also available for your use. Selectable as a boot action or from within Setup, it can present HTML files to your end users to document the platform, provide contact information for your company, etc. This provides a convenient means of providing information to help users recover from hardware problems, like a failed hard drive.

Also available is a password protection system, so that a password must be provided by the end-user before POST allows booting of an operating system. The password is stored in CMOS, is one-way encrypted, and can be modified in a setup screen.

The ability to shadow slower ROM devices with DRAM or SRAM is selectable in the shadow setup screen and calls chipset-specific code to enable shadowing for the BIOS ROM itself or for feature ROMs on a 16 Kbyte region basis. DRAM may take the form of FP, EDO, SDRAM, RDRAM, or other technologies.

Embedded BIOS provides extensive support for both internal CPU cache control (i486 and above) and external cache control (typically chipset-controlled). Internal cache is managed by the CPU class personality modules, whereas external cache is managed by the cache manager, which directs peripherals (chipset, 8042, custom I/O ports, and/or CPU integrated peripherals) to manage the cache. Keyboard controls on the PC/AT keyboard are implemented for enabling and disabling the cache on the fly (while the system is running). The BIOS provides cache control services to applications that allow operating systems and user code to control and inspect the status of the cache.

CPU speed controls are handled by the system BIOS by routing control through the appropriate logic (chipset, 8042, custom I/O ports, and/or CPU integrated peripherals). As with cache control, CPU speed is controllable on the fly at the keyboard or via programming interfaces.

6.1.3 Software Compatibility

Embedded BIOS offers a high degree of compatibility with past and current BIOS standards, allowing it to run off-the-shelf operating system software and application software.

Embedded BIOS has been tested with all industry-standard operating systems, including versions of Windows, Linux, DOS, and real time operating systems.

Embedded BIOS is rigorously tested with programs such as AMI Diag, MSD, Check-It, Manifest and Q/A Plus, ensuring its compatibility with established desktop application standards.

In addition to its standard data structures and programming interfaces, Embedded BIOS provides support for industry-standard initiatives, including ACPI, APM, El Torito, Legacy USB, MP, PCI, PMM, PXE, and SMBIOS (formerly DMI).

6.2 BIOS User Interface

6.2.1 Power On Self Test (POST)

When the evaluation board is powered on, Embedded BIOS tests and initializes the hardware and programs the chipset and other peripheral components. During this time, POST progress codes are written by the system BIOS to I/O port 80h, allowing the user to monitor the progress with a special monitor. Section 6.8 lists the POST codes and their meanings.

During early POST, no video is available to display error messages should a critical error be encountered; therefore, POST uses beeps on the speaker to indicate the failure of a critical system component during this time. Consult Section 6.9 for a list of Beep codes used by the evaluation board's BIOS.

6.2.2 The BIOS User Interface

The evaluation board BIOS can use the standard keyboard and video device, or use console redirection to demonstrate headless operation. For headless operation, remove the keyboard and screen device and the system will boot unattended. If an RS232 cable is attached to COM1, a PC/AT-style character-based POST is available from HyperTerminal, PROCOMM, or any other terminal emulator software that supports VT100 emulation.

When a keyboard and video device are attached, the evaluation board can display either a traditional character-based PC BIOS display with memory count-up, or it can display a graphical POST with splash screen and progress icons. Both POST displays accept a <DEL> key press to enter the setup screen, and both display boot-time progress activity displays. The graphical display shows the status of file system devices and even OEM-defined devices (when the OEM adapts the BIOS to a particular OEM platform), but omits character-based PCI resource display. The text-based POST displays the memory count-up and the PCI resource assignment table.

Figure 9 shows the format of the text-based POST display. The display is very similar if console redirection through a COM port is used instead (this feature is discussed later in this manual).

Figure 9. Text-based POST Display

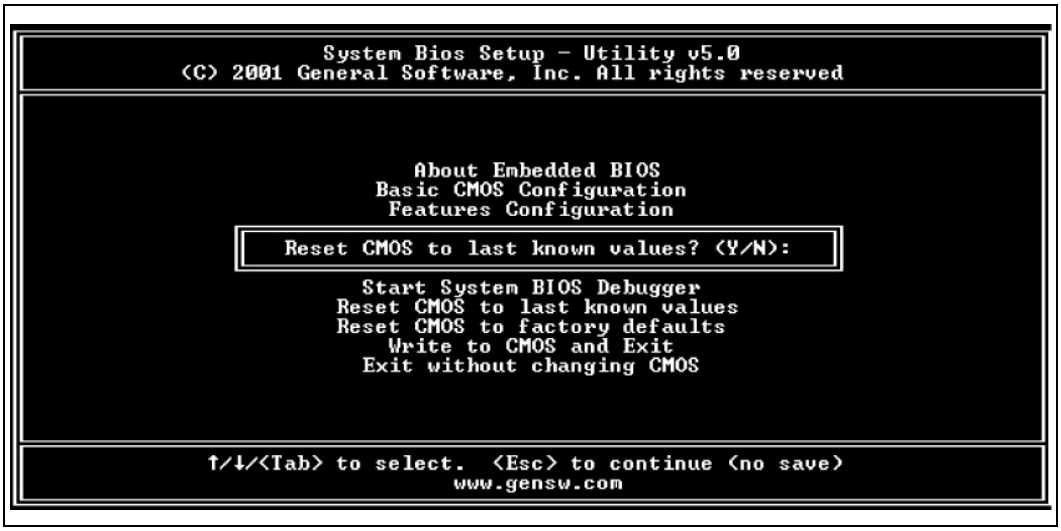
Figure 10 shows the graphical version of POST. The BIOS decompresses the main image, and can display multiple overlaid graphics at various points in POST. The OEM can define the entire sequence and control the timing of the system for an embedded application, and can arrange to have different graphics displayed on each successive boot of the system. This feature is ideal for embedded systems that must show evidence of operation during startup, while the application loads underneath the splash screen. Once the application begins writing to the screen, the splash screen relinquishes control, providing a seamless graphical progression for the end user.

Figure 10. Graphical POST

When the evaluation board is powered on for the first time, you'll need to configure the system through the Setup Screen System (described later) before peripherals, such as disk drives, are recognized by the BIOS. The information is written to battery-backed CMOS RAM on the board's Real Time Clock. Should the board's battery fail, this information will be lost and the board will need to be reconfigured.

The evaluation board's Basic Setup Screen provides an option to disable the graphical POST and switch to the legacy text-based version. This feature may not permanently disable the graphical POST if the BIOS adaptation calls for reverting to the graphical form after so many boots. If you find that the graphical POST comes back after several boots, it is because this option is enabled for this platform. Naturally, the OEM can use the Embedded BIOS Adaptation Kit to control whether setup can be used to dictate the policy, and whether it is permanent or temporary.

Figure 11. Embedded BIOS Setup Screen

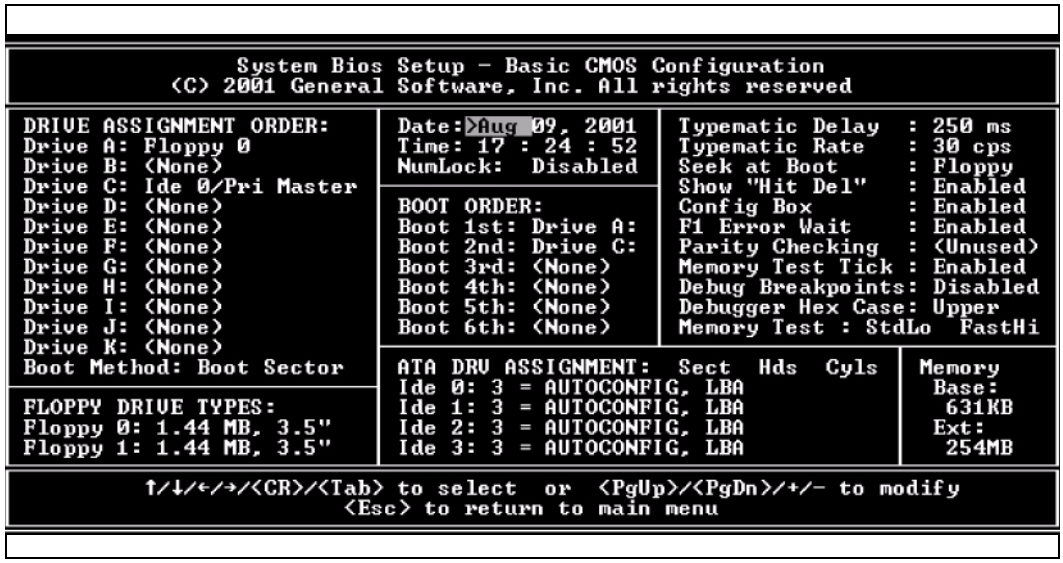


Once in the Setup Screen System (Figure 11), the user can navigate with the UP and DOWN arrow keys from the main console or use the Ctrl E (^E) and Ctrl X (^X) keys from the remote terminal program to accomplish the same thing. TAB and ENTER are used to advance to the next field, and '+' and '-' keys cycle through values, such as those in the Basic Setup Screen or the Diagnostics Setup Screen.

6.2.3 Basic CMOS Configuration Screen

The evaluation board's drive types, boot activities, and POST optimizations are configured from the Basic Setup Screen (Figure 12). To use disk drives with your system, you must select appropriate assignments of drive types in the left-hand column. Then, if you are using true floppy and IDE drives (not memory disks that emulate these drives), you need to configure the drive types themselves in the Floppy Drive Types and IDE Drive Geometry sections. Finally, you'll need to configure the boot sequence in the middle of the screen. Once these selections have been made, your system is ready to use.

Figure 12. Embedded BIOS Basic Setup Screen



6.2.4 Configuring Drive Assignments

Embedded BIOS allows the user to map a different file system to each drive letter. The BIOS allows file systems for each floppy (Floppy0 and Floppy1), each IDE drive (Ide0, Ide1, Ide2, and Ide3). Figure 12 shows how the first floppy drive (Floppy0) is assigned to drive A: in the system, and then shows how the first IDE drive (Ide0) is assigned to drive C: in the system.

Caution: Take care to not skip drive A: when making floppy disk assignments, as well as drive C: when making hard disk assignments. The first floppy should be A:, and the first hard drive should be C:. Also, do not assign the same file system to more than one drive letter. Thus, Floppy0 should not be used for both A: and B:. The BIOS permits this to allow embedded devices to alias drives, but desktop operating systems may not be able to maintain cache coherency with such a mapping in place.

6.2.5 Configuring Floppy Drive Types

If true floppy drive file systems (and not their emulators, such as ROM, RAM, or Flash disks) are mapped to drive letters, then the floppy drives themselves must be configured in this section. Floppy0 refers to the first floppy disk drive on the drive ribbon cable (normally drive A:), and Floppy1 refers to the second drive (drive B:).

6.2.6 Configuring IDE Drive Types

If true IDE disk file systems (and not their emulators, such as ROM, RAM, or Flash disks) are mapped to drive letters, then the IDE drives themselves must be configured in this section. The list shows the drive assignments for Ide0-Ide3:

File System NameControllerMaster/Slave

Ide0Primary (1f0h)Master

Ide1Primary (1f0h)Slave

Ide2Secondary (170h)Master

Ide3Secondary (170h)Slave

To use the primary master IDE drive in your system (the typical case), just configure Ide0 in this section, and map Ide0 to drive C: in the Configuring Drive Assignments section.

The IDE Drive Types section lets you select the type for each of the four IDE drives: None, User, Physical, LBA, or CHS.

The **User** type allows the user to select the maximum cylinders, heads, and sectors per track associated with the IDE drive. This method is now rarely used since LBA is now in common use.

The **Physical** type instructs the BIOS to query the drive's geometry from the controller on each POST. No translation on the drive's geometry is performed, so this type is limited to drives of 512 Mbytes or less. Commonly, this is used with embedded ATA PC Cards.

The **LBA** type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translates the geometry according to the industry-standard LBA convention. This supports up to 128 Gbyte drives. ***Use this method for all new drives.***

The **CHS** type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translates the geometry according to the Phoenix CHS convention. Using this type on a drive previously formatted with LBA or physical geometry might show data as being missing or corrupted.

6.2.7 Boot Device Configuration

Embedded BIOS supports user-defined steps in the boot sequence. When the entire system has been initialized, POST executes these steps in order until an operating system successfully loads. In addition, other pre-boot features can be run before, after, or between operating system load attempts. The following actions are supported:

- **Drive A: - D:** Boot operating system from specified drive. If "Loader" is set to "BootRecord" or "Unused", then the standard boot record will be invoked, causing any industry-standard operating system to load. If "Boot Method" is set to "Windows CE" then the boot drive's boot

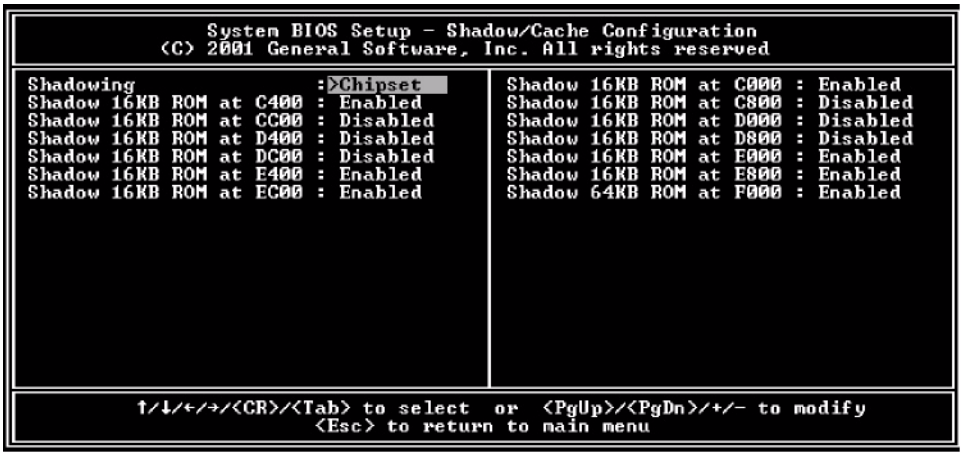
record will not be used, and instead the BIOS will attempt to load and execute the Windows CE kernel file, NK.BIN, from the root directory of each boot device.

- **CDROM:** Boot from the first IDE CDROM found that contains an El Torito bootable CDROM.
- **Debugger:** Launch the integrated BIOS dbugger. To exit the debugger environment, type “G” at the debugger prompt and press ENTER.
- **Browser:** Launch the integrated HTML browser. The browser allows the user to navigate through HTML formatted information (contained within the BIOS ROM) about the platform, about General Software, and related topics. To return from the browser environment, simply press ESC at the top level browser screen.
- **MFGMODE:** Initiate Manufacturing Mode, allowing the system to be configured remotely via an RS232 connection to a host computer.
- **DOS in ROM:** Execute a ROM-resident copy of DOS, if available. This feature is not applicable unless an XIP copy of DOS has been stored in the BIOS boot ROM.
- **Alarm:** Generate an alarm by beeping the speaker and sending a signal to a Firmware Application running in the Firmbase environment. The application can perform whatever processing is necessary to handle the alarm, including taking local action, interacting with other tightly coupled computers, or even notifying other systems on the network, for example. These applications are beyond the scope of the Embedded BIOS Adaptation Kit.
- **RAS:** Enter remote access mode by sending a signal to a firmware application running in the firmbase environment. The application can perform whatever processing is necessary to implement the RAS mode, which is largely defined to mean some state where the system accepts remote connections for normal operation; not specifically for field maintenance. These applications are beyond the scope of the Embedded BIOS Adaptation Kit.
- **Power Off:** Cause the evaluation board to switch off its power with a “soft off” feature, and signal firmware applications running in the Firmbase environment that power is going down. These applications are beyond the scope of the Embedded BIOS Adaptation Kit.
- **Reboot:** Reboot the evaluation board, and send a signal to a Firmware Application running in the Firmbase environment indicating that the evaluation board is rebooting. These applications are beyond the scope of the Embedded BIOS Adaptation Kit.
- **CLI:** Enter command line mode by calling a special Board Module Function (BoardPostControl) that can be used to implement an OEM-defined Command Language Interpreter. The design of such an interpreter is beyond the scope of the Embedded BIOS Adaptation Kit.
- **None:** No action; POST proceeds to the next activity in the sequence.

6.2.8 Shadow Configuration Setup Screen

The evaluation board’s Shadow Configuration Setup Screen (Figure 13) allows selective enabling and disabling of shadowing in 16KB sections, except for the top 64KB of the BIOS ROM, which is shadowed as a unit. Normally, shadowing should be enabled at C000/C400 (to enhance VGA ROM BIOS performance) and E000-F000 should be shadowed to maximize system ROM BIOS performance.

Figure 13. Embedded BIOS Shadow Setup Screen

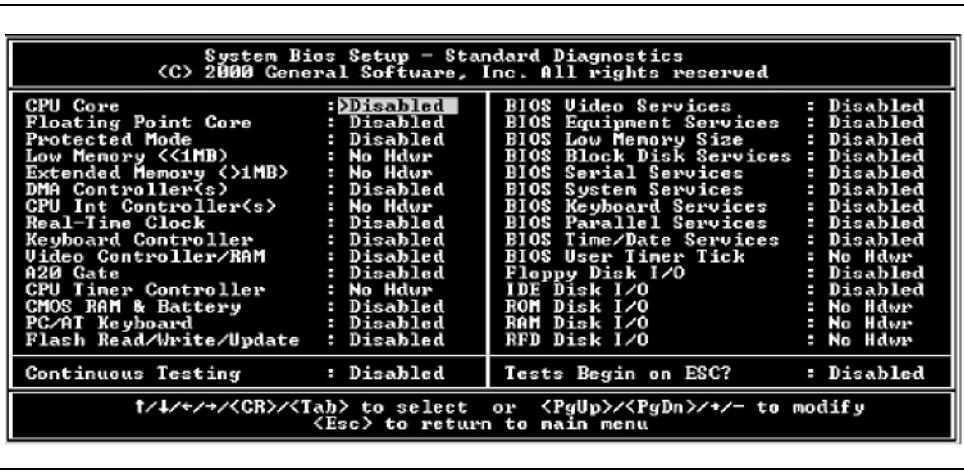


Embedded systems may require automated burn-in testing in the development cycle. This facility is provided directly in the evaluation board's system BIOS through the Standard Diagnostics Routines Setup Screen (Figure 14). To use the system, selectively enable or disable features to be tested, and then enable the "Tests Begin on ESC?" option to cause the system test suite to be invoked. To repeat the system test battery continuously, you should also enable the "Continuous Testing" option. When continuous testing is started, the system will continue until an error is encountered.

Caution: The disk I/O diagnostics perform write operations on those drives; therefore, only spare drives should be used which do not contain data that could be harmed by the test.

Note: The keyboard test may fail when in fact the hardware is operating within reasonable limits. This is because although the device may produce occasional errors, the BIOS retries operations when failures occur during normal operation of the system.

Figure 14. Standard Diagnostic Routines Setup Screen



6.2.9 Start System BIOS Debugger Setup Screen

The Embedded BIOS Integrated Debugger may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, the debugger will display the debugger prompt:

EBDEBUG:

and await debugger commands. To resume back to the Setup Screen main menu, type the following command, which instructs the debugger to “go”:

EBDEBUG: **G** (ENTER)

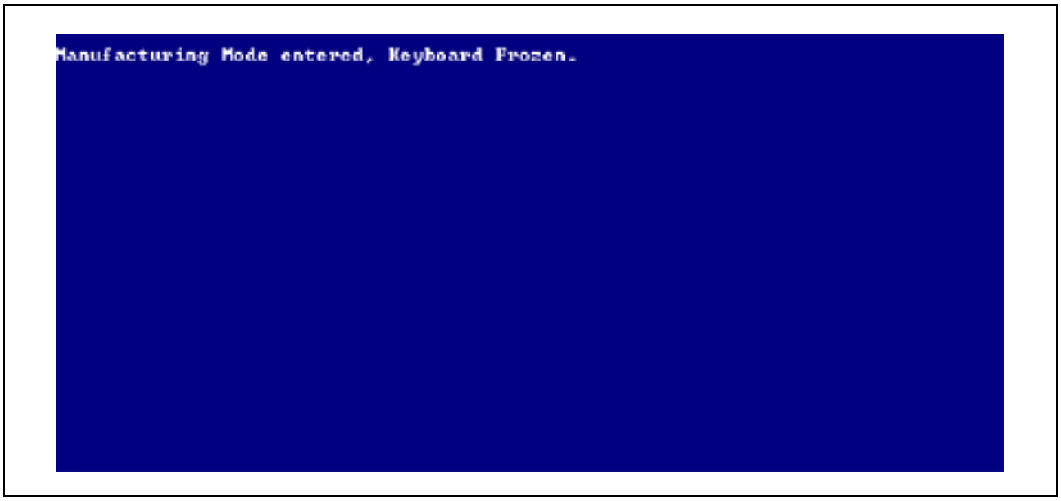
On multiprocessing systems (those with more than one CPU), the debugger can be used to run commands on different CPUs. When the system detects multiple processors, the debugger’s prompt changes to indicate which CPU performs the debugger’s commands as they are typed. The multiprocessor prompt is shown below (using CPU 2 as an example):

EBDEBUG [2]:

6.2.10 Start RS232 Manufacturing Link Setup Screen

The Embedded BIOS Manufacturing Mode may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, Manufacturing Mode takes over the system and freezes the system console (Figure 15). The host can resume operation of the system and give control back to the evaluation board Setup Screen system with special control software.

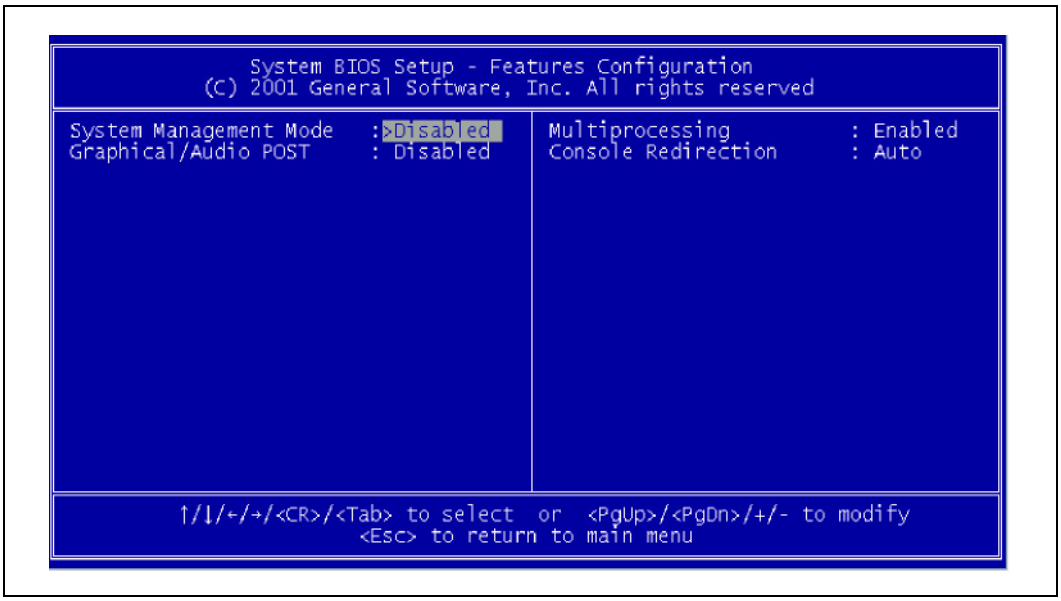
Figure 15. Start RS232 Manufacturing Link Setup Screen



6.2.11 Enabling and Disabling Run-Time System BIOS Features

The Embedded BIOS Features Setup screen can be used to enable or disable certain features of this platform. Figure 16 shows an example Features Setup screen. It should be noted that this screen may vary from target to target, based on what features were enabled at the time the BIOS was built for this platform. Features that can be controlled with this screen include ACPI, Console Redirection, Multiprocessing, PnP, PnP OS, PMM, SMBIOS.

Figure 16. Features Setup Screen



6.3 Manufacturing Mode

The evaluation board's BIOS may provide a special mode, called Manufacturing Mode, which allows the evaluation board to be controlled by a host computer such as a laptop or desktop PC. Running special software supplied by General Software, the host can access the evaluation board's drives and manage the file systems on the evaluation board, reprogram Flash memories, and test the evaluation board hardware.

There are several methods by which the evaluation board can enter Manufacturing Mode. These methods are detailed elsewhere in this manual and others.

Once the evaluation board has entered Manufacturing Mode, the host PC may cause the evaluation board to perform functions by issuing commands in protocol over the RS-232 connection. There are two ways to access the evaluation board from the host PC.

6.3.1 Sample Manufacturing Mode HOST Program

The first way to access the evaluation board from the host PC is to run a program that accesses the host-side Manufacturing Mode functions. An example of such a program is `HOST.EXE`, which can be obtained from General Software. This program runs under DOS and, using a full-screen

windowing interface, illustrates the basic functionality of the Manufacturing Mode protocol. It should be noted that this program is a working example program, and is not intended to be a production-quality control tool.

Run the HOST program on a "host" computer, so that its main menu is displayed. By default HOST connects via COM1 (3F8h). The default baud rate is set to "auto," meaning it will use whatever baud rate the evaluation board is set to. You can change both of these by using command line switches. Type "HOST /?" for the available switches.

On the host, select **GET HOST ATTENTION**, within a couple seconds of selecting the manufacturing mode on the evaluation board. You should see the host program immediately display a yellow status box that shows that the connection has been established.

If the connection hasn't been established, then try the connection again on the host side, or reboot the evaluation board and try again, this time having the host program get the evaluation board's attention within two seconds or so of the evaluation board's entering of manufacturing mode. If this still fails, check that your null modem serial cable is connected securely to the proper ports. You may also want to lower the baud rate for the manufacturing mode on the evaluation board, since a higher baud rate may be more error prone.

Once you have established a connection, you can use HOST to test the link by continuously exercising it, or scanning the evaluation board's drives, or uploading files in Flash, and more.

6.3.2 Manufacturing Mode Drive Redirection

The second way to access the evaluation board through Manufacturing Mode is to install the `MFGDRV.SYS` device driver on the host system. This device driver loads under MS-DOS and Windows 98 DOS mode, and maps a new drive letter on the host to a drive on the evaluation board. It is a DOS-only driver, and will not operate under Linux or Windows, not even in a Windows DOS box.

The INT 13h redirection support in the Manufacturing Mode protocol can be exposed by loading the `MFGDRV.SYS` device driver on the host by using the following `CONFIG.SYS` line:

```
DEVICE=MFGDRV.SYS /BAUD=rate /PORT=COMn /UNIT=u /AUTO
```

This device driver runs under any DOS-compatible operating system, and creates a drive letter on your host PC (usually D: if your last hard drive is C:) that can be used to interact with the specified INT 13h unit.

The *u* parameter specifies the BIOS unit number of the floppy disk, RAM disk, RFD drive, or ROM disk to be redirected, where 0 corresponds to drive A: and 1 for drive B. By default, this value is 80 (a hex number without a "0x" in front or 'h' appended to it), which corresponds with the unit for the first hard drive or emulator.

The `/BAUD=rate` parameter can be used to match the baud rate used by the evaluation board's BIOS. Legal values are 19K, 28K, 38K, 56K, and 115K. If this parameter is not specified, then the baud rate is autodetected.

The `/AUTO` parameter, if specified, tells `MFGDRV.SYS` to automatically format the remote drive if it determines that it is unformatted. By default, `MFGDRV.SYS` will not automatically format the remote drive, and will instead examine the media for a pre-existing format. If not found, then `MFGDRV.SYS` asks the host PC operator if the remote drive should be formatted.

Once the connection is established, you can read and write the evaluation board's drive as if it were simply another drive on your host system. The only difference is that it will be a bit slower over the serial connection.

Note: `MFGDRV.SYS` assumes that other software does not reprogram the COM port being used on the host for its purposes, and that it has exclusive access to it. If you run other software, such as terminal emulation programs, they may disable the COM port UART, causing `MFGDRV.SYS` to appear to stop working. It is best to avoid running such software on the host when `MFGDRV.SYS` is loaded. Note: `HOST.EXE` is an example of such a program, since it takes over the UART for its own purposes. If you run `HOST.EXE` when `MFGDRV.SYS` is loaded, you must reboot the host PC for the `MFGDRV.SYS` driver to reestablish its control over the UART.

A full discussion of the uses of Manufacturing Mode is beyond the scope of this manual. Complete documentation and host-side software is available directly from General Software. For more information, visit the General Software web site at www.gensw.com.

6.4 Console Redirection

The evaluation board can operate either with a standard PC/AT or PS/2 keyboard and VGA video monitor, or with a special emulation of a console over an RS232 cable connected to a host computer running a terminal program. To see an example session with Hyperterminal, see Figure 17, "Integrated BIOS Debugger" on page 73.

To use the Console Redirection feature, simply connected the target to a host computer running a communications program running at 9600 baud (this slower baud rate was chosen as a default for demonstration BIOS binaries, but can be changed with the Embedded BIOS Adaptation Kit.) Then, reboot the target.

The target makes three checks during POST to determine if console redirection should be enabled, or if the default video system (if any) should be used. First, if a cable is not connected to a booted host, then it does not use console redirection. Second, if a cable is detected, then if the communication program is not running, it does not enable console redirection. Finally, if the communication program is running with the cable connected, POST requires the user to type any of three characters (ESC, ENTER/CR, or ^C). It is recommended that the remote user using console redirection press one of these characters several times during POST (well before video appears) so that the character is received after the power supply has come up but before the POST tests are performed.

If the user presses ESC during this test on the remote console, then POST begins console redirection, and uses the ESC as it would an ESC type-in on the main console, to indicate that it should accelerate the memory test and boot the system more quickly.

If the user presses ENTER (or CR) during this test on the remote console, then POST begins console redirection, and does not otherwise use the key press.

If the user presses ^C during this test on the remote console, then POST begins console redirection, and uses the ^C as it would a ^C type-in on the main console, to indicate that it should enter the Setup screen before booting the target.

The software on the HOST can be any terminal emulation program that supports ANSI terminal mode, using 9600 baud, no parity, and one stop bit (Note: This can be modified by the OEM during BIOS adaptation.) The program must be set to not use flow control, or the console may seem to

stall or not accept input.

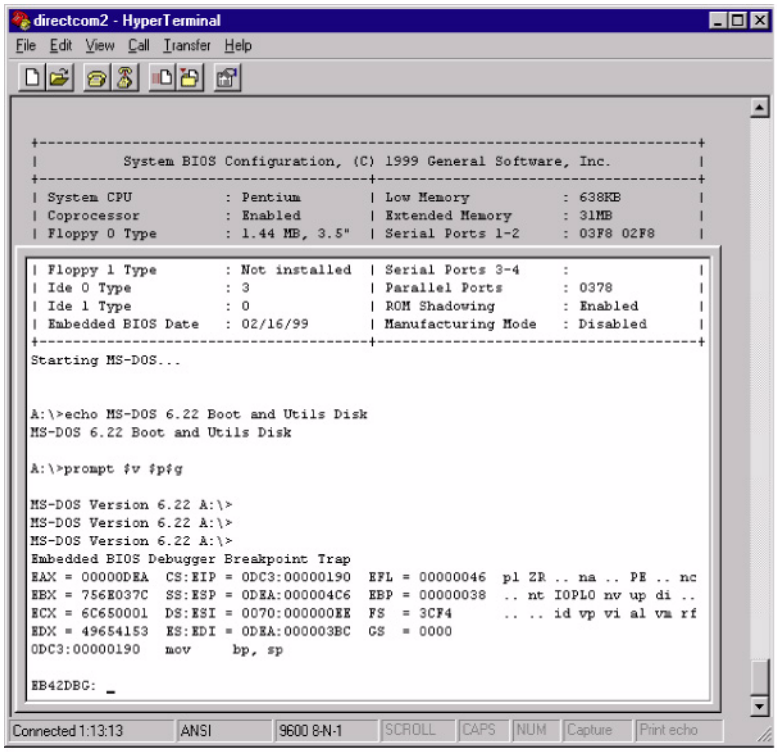
Caution: Hyper Terminal's default setting is to use flow control, which will render the console inoperative. To change this, create a new session, change the flow control setting to "none", save the session, and exit Hyper Terminal. Then reinvoke Hyper Terminal with the session and it will operate with the new flow control setting.

6.5 Integrated BIOS Debugger

The evaluation board's BIOS contains a built-in debugger that can be a valuable tool to aid the board bring-up process on new designs similar to the reference board. It supports a DOS SYMDEB-style command line interface, and can be used on the main console's keyboard and screen, or over a redirected connection to a terminal program (see Section 6.4).

To activate the debugger at any time from the main console, press the left shift and the control keys together. A display similar to the one in the Hyper Terminal session below (Figure 17) will appear, containing the title, "Embedded BIOS Debugger Breakpoint Trap" and a snapshot of the CPU general registers.

Figure 17. Integrated BIOS Debugger



To leave the debugger and resume the interrupted activity (whether POST, BIOS, DOS, Windows, or an application program), enter the "G" command (short for "go") and press ENTER. If you were at a DOS prompt when you entered the debugger, then DOS will still be waiting for its command, and will not prompt again until you press ENTER again.

The debugger can also be entered from the Setup Screen System, and as a boot activity (see Figure 12), as a last ditch effort during board bring-up and development if no bootable device is available.

If your version of DOS, an application, or any OEM-supplied BIOS extensions have debugging code (i.e., “INT 3” instructions) remaining, then these will invoke the debugger automatically, although this is not an error. To continue, use the “G” command. When Embedded BIOS is adapted by the OEM, the debugger can be removed from the final production BIOS, and superfluous debugging code in the application will not cause the debugger to be invoked.

A complete discussion of the debugger is beyond the scope of this chapter; however, complete documentation is available from General Software.

6.6 Integrated HTML Browser

The evaluation board’s BIOS contains a built-in HTML browser that allows the user to browse (in text mode using the keyboard instead of the mouse) HTML documents stored in the BIOS ROM.

The HTML browser can be a boot action item, and by default is the primary boot action. Thus, when a platform boots for the first time, it should cause the browser to display its first page. The HTML pages for a platform are created using the Embedded BIOS Adaptation Kit. The ones for this platform were designed to provide the user with information about the platform, about General Software, about the firmware, and how to obtain technical support for the platform.

General Software ODM/OEM customers can use the Embedded BIOS Adaptation Kit to create their own HTML user interface to their embedded device, simply by writing HTML. The HTML browser works over the main console, and over console redirection as well.

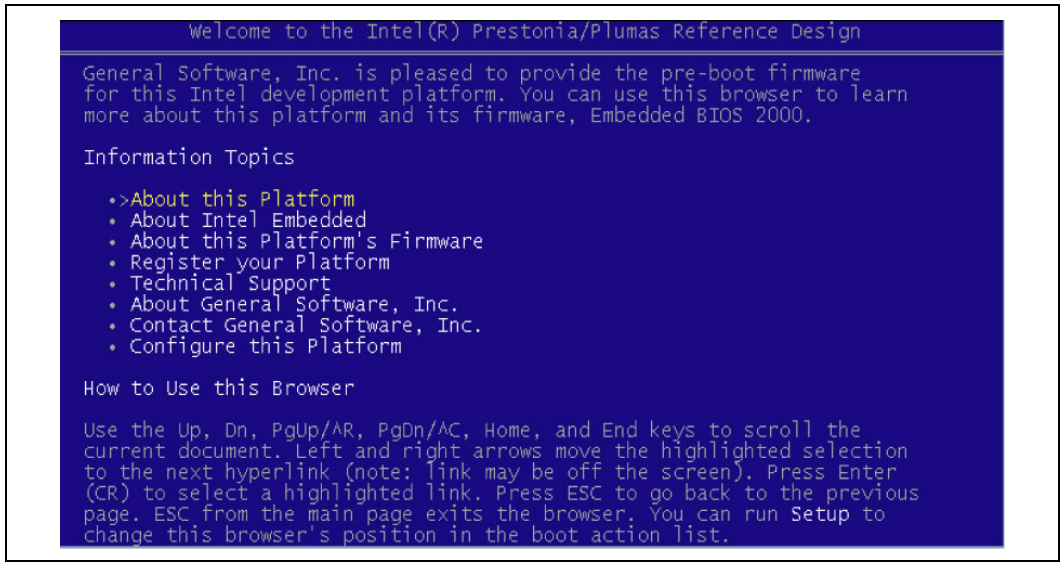
The main page (Figure 18) is automatically displayed when the browser is invoked. To exit a page and go to a previous page (or from the main page, to exit the browser), simply press the ESC key.

To scroll up and down, use the Up and Down arrow keys on your keypad (making sure NumLock is turned off in order for these keys to work). To advance the cursor to the previous or next hyperlink (highlighted in a different color), use the Left and Right arrow keys on you keypad. You may also use the PgUp, PgDn, Home, and End keys to navigate the current page.

To select the hyperlink under the cursor, press ENTER. This will cause the new page to be displayed. To get back to the previous page, press ESC.

The browser can display HTML text, and can also invoke BIOS functionality (and even cause OEM code to be executed) with special embedded targets. This is demonstrated in the demonstration HTML for this platform, allowing the user to enter the Setup screen and perform other maintenance functions from within the browser's display.

Figure 18. Integrated HTML Browser



A complete discussion of the browser, including the limited set of HTML supported, is beyond the scope of this chapter; however, complete documentation is available from General Software.

6.7 System Registration

The evaluation board's BIOS incorporates a system registration facility that provides a method for users to obtain technical support from General Software directly. As the supplier of the BIOS for this platform, and as a supplier of Embedded BIOS Adaptation Kit products that ODMs and OEMs can use to build perfect-fit BIOSes for their own designs, General Software is ideally positioned to provide the technical support that embedded ODM/OEM users of this board need. There is no cost to registered users for this support.

Registration of this system provides two important benefits. The first is access to General Software's technical support services. The second is to reduce boot-time delay, resulting in a faster system during startup.

To register your system, enter the Setup main menu and select Register System. Then follow the directions on that screen (see Figure 19). This screen will display your system's ID, which should be copied down and then entered into General Software's on-line registration web page (see Figure 20).

Figure 19. Registration Screen

To obtain the registration key associated with your system, visit General Software's Internet web site for registrations at http://www.gensw.com/register. You should see a page similar to that shown in Figure 20.

To receive your registration key and be eligible to receive technical support from General Software, you must supply basic contact information on the web site, including your e-mail address. General Software does not provide this information to third parties, but uses it internally to qualify you for support.

Once you submit the information on this form, a General Software registration server will email your registration key back to you, to the e-mail address you specified when you registered.

If you are unable to use the on-line registration system, email General Software at sales@gensw.com, or contact them by telephone at (425) 576-8300.

Figure 20. General Software's Registration Web site

Some users of this platform (such as Field Application Engineers or Sales Engineers) may loan the system to other people. General Software encourages the person loaning the system to another person to deregister the system by going into the Setup screen and selecting Deregister System. This removes their email address from the system's sign-on banner, and encourages the person receiving the board to register the system so they may receive support from General Software. If the system moves on to another person, or back to the original person, General Software encourages re-registration of the system so that the system is always supported.

6.8 Embedded BIOS POST Codes

Embedded BIOS writes progress codes, also known as POST codes, to I/O port 80h during POST, in order to provide information to OEM developers about system faults. These POST codes may be monitored by a port 80h card in either an ISA slot or PCI slot; they are not displayed on the screen. For more information about POST codes, contact General Software. Please note that the Embedded BIOS adaptation may be configured to reroute these codes over another I/O port or device.

Mnemonic Code	Code	System Progress Report
POST_STATUS_START	00h	Start POST (BIOS is executing).
POST_STATUS_CPUTEST	01h	Start CPU register test.
POST_STATUS_DELAY	02h	Start power-on delay.
POST_STATUS_DELAYDONE	03h	Power-on delay finished.
POST_STATUS_KBDBATRDY	04h	Keyboard BAT finished.
POST_STATUS_DISABSHADOW	05h	Disable shadowing & cache.
POST_STATUS_CALCCKSUM	06h	Compute ROM CRC, wait for KBC.
POST_STATUS_CKSUMGOOD	07h	CRC okay, KBC ready.
POST_STATUS_BATVRFY	08h	Verifying BAT command to KB.
POST_STATUS_KBDCMD	09h	Start KBC command.
POST_STATUS_KBDDATA	0ah	Start KBC data.
POST_STATUS_BLKUNBLK	0bh	Start pin 23,24 blocking & unblocking.
POST_STATUS_KBDNOP	0ch	Start KBC NOP command.
POST_STATUS_SHUTTEST	0dh	Test CMOS RAM shutdown register.
POST_STATUS_CMOSDIAG	0eh	Check CMOS checksum.
POST_STATUS_CMOSINIT	0fh	Initialize CMOS contents.
POST_STATUS_CMOSSTATUS	10h	Initialize CMOS status for date/time.
POST_STATUS_DISABDMAINT	11h	Disable DMA, PICs.
POST_STATUS_DISABPORTB	12h	Disable Port B, video display.
POST_STATUS_BOARD	13h	Initialize board, start memory detection.
POST_STATUS_TESTTIMER	14h	Start timer tests.
POST_STATUS_TESTTIMER2	15h	Test 8254 T2, for speaker, port B.
POST_STATUS_TESTTIMER1	16h	Test 8254 T1, for refresh.
POST_STATUS_TESTTIMER0	17h	Test 8254 T0, for 18.2Hz.
POST_STATUS_MEMREFRESH	18h	Start memory refresh.
POST_STATUS_TESTREFRESH	19h	Test memory refresh.
POST_STATUS_TEST15US	1ah	Test 15usec refresh ON/OFF time.
POST_STATUS_TEST64KB	1bh	Test base 64KB memory.
POST_STATUS_TESTDATA	1ch	Test data lines.
POST_STATUS_TESTADDR	20h	Test address lines.
POST_STATUS_TESTPARITY	21h	Test parity (toggling).
POST_STATUS_TESTMEMRDWR	22h	Test Base 64KB memory.
POST_STATUS_SYSINIT	23h	Prepare system for IVT initialization.
POST_STATUS_INITVECTORS	24h	Initialize vector table.
POST_STATUS_8042TURBO	25h	Read 8042 for turbo switch setting.
POST_STATUS_POSTTURBO	26h	Initialize turbo data.
POST_STATUS_POSTVECTORS	27h	Modification of IVT.

POST_STATUS_MONOMODE	28h	Video in monochrome mode verified.
POST_STATUS_COLORMODE	29h	Video in color mode verified.
POST_STATUS_TOGGLEPARITY	2ah	Toggle parity before video ROM test.
POST_STATUS_INITBEFOREVIDEO	2bh	Initialize before video ROM check.
POST_STATUS_VIDEOROM	2ch	Passing control to video ROM.
POST_STATUS_POSTVIDEO	2dh	Control returned from video ROM.
POST_STATUS_CHECKEGAVGA	2eh	Check for EGA/VGA adapter.
POST_STATUS_TESTVIDEOMEMORY	2fh	No EGA/VGA found, test video memory.
POST_STATUS_RETRACE	30h	Scan for video retrace signal.
POST_STATUS_ALTDISPLAY	31h	Primary retrace failed.
POST_STATUS_ALTRETRACE	32h	Alternate found.
POST_STATUS_VRFYSWADAPTER	33h	Verify video switches.
POST_STATUS_SETDISPMODE	34h	Establish display mode.
POST_STATUS_CHECKSEG40A	35h	Initialize ROM BIOS data area.
POST_STATUS_SETCURSOR	36h	Set cursor for power-on msg.
POST_STATUS_PWRONDISPLAY	37h	Display power-on message.
POST_STATUS_SAVECURSOR	38h	Save cursor position.
POST_STATUS_BIOSIDENT	39h	Display BIOS identification string.
POST_STATUS_HITDEL	3ah	Display “Hit <DEL> to ...” message.
POST_STATUS_VIRTUAL	40h	Prepare protected mode test.
POST_STATUS_DESCR	41h	Prepare descriptor tables.
POST_STATUS_ENTERVM	42h	Enter virtual mode for memory test.
POST_STATUS_ENABINT	43h	Enable interrupts for diagnostics mode.
POST_STATUS_CHECKWRAP1	44h	Initialize data for memory wrap test.
POST_STATUS_CHECKWRAP2	45h	Test for wrap, find total memory size.
POST_STATUS_HIGHPATTERNS	46h	Write extended memory test patterns.
POST_STATUS_LOWPATTERNS	47h	Write conventional memory test patterns.
POST_STATUS_FINDLOWMEM	48h	Find low memory size from patterns.
POST_STATUS_FINDHIMEM	49h	Find high memory size from patterns.
POST_STATUS_CHECKSEG40B	4ah	Verify ROM BIOS data area again.
POST_STATUS_CHECKDEL	4bh	Check for <DEL> pressed.
POST_STATUS_CLREXTMEM	4ch	Clear extended memory for soft reset.
POST_STATUS_SAVEMEMSIZE	4dh	Save memory size.
POST_STATUS_COLD64TEST	4eh	Cold boot: Display 1st 64KB memtest.
POST_STATUS_COLDLOWTEST	4fh	Cold boot: Test all of low memory.
POST_STATUS_ADJUSTLOW	50h	Adjust memory size for EBDA usage.
POST_STATUS_COLDHITEST	51h	Cold boot: Test high memory.
POST_STATUS_REALMODETEST	52h	Prepare for shutdown to real mode.
POST_STATUS_ENTERREAL	53h	Return to real mode.
POST_STATUS_SHUTDOWN	54h	Shutdown successful.
POST_STATUS_DISABA20	55h	Disable A20 line.
POST_STATUS_CHECKSEG40C	56h	Check ROM BIOS data area again.
POST_STATUS_CHECKSEG40D	57h	Check ROM BIOS data area again.
POST_STATUS_CLRHITDEL	58h	Clear “Hit <DEL>“ message.
POST_STATUS_TESTDMAPAGE	59h	Test DMA page register file.
POST_STATUS_VRFYDISPMEM	60h	Verify from display memory.

POST_STATUS_TESTDMA0BASE	61h	Test DMA0 base register.
POST_STATUS_TESTDMA1BASE	62h	Test DMA1 base register.
POST_STATUS_CHECKSEG40E	63h	Checking ROM BIOS data area again.
POST_STATUS_CHECKSEG40F	64h	Checking ROM BIOS data area again.
POST_STATUS_PROGDMA	65h	Program DMA controllers.
POST_STATUS_INITINTCTRL	66h	Initialize PICs.
POST_STATUS_STARTKBDTEST	67h	Start keyboard test.
POST_STATUS_KBDRESET	80h	Issue KB reset command.
POST_STATUS_CHECKSTUCKKEYS	81h	Check for stuck keys.
POST_STATUS_INITCIRCBUFFER	82h	Initialize circular buffer.
POST_STATUS_CHECKLOCKEDKEYS	83h	Check for locked keys.
POST_STATUS_MEMSIZEMISMATCH	84h	Check for memory size mismatch.
POST_STATUS_PASSWORD	85h	Check for password or bypass setup.
POST_STATUS_BEFORESETUP	86h	Password accepted.
POST_STATUS_CALLSETUP	87h	Entering setup system.
POST_STATUS_POSTSETUP	88h	Setup system exited.
POST_STATUS_DISPPWRON	89h	Display power-on screen message.
POST_STATUS_DISPWAIT	8ah	Display “Wait...” message.
POST_STATUS_ENABSHADOW	8bh	Shadow system & video BIOS.
POST_STATUS_STDCMOSSETUP	8ch	Load standard setup values from CMOS.
POST_STATUS_MOUSE	8dh	Test and initialize mouse.
POST_STATUS_FLOPPY	8eh	Test floppy disks.
POST_STATUS_CONFIGFLOPPY	8fh	Configure floppy drives.
POST_STATUS_IDE	90h	Test hard disks.
POST_STATUS_CONFIGIDE	91h	Configure IDE drives.
POST_STATUS_CHECKSEG40G	92h	Checking ROM BIOS data area.
POST_STATUS_CHECKSEG40H	93h	Checking ROM BIOS data area.
POST_STATUS_SETMEMSIZE	94h	Set base & extended memory sizes.
POST_STATUS_SIZEADJUST	95h	Adjust low memory size for EBDA.
POST_STATUS_INITC8000	96h	Initialize before calling C800h ROM.
POST_STATUS_CALLC8000	97h	Call ROM BIOS extension at C800h.
POST_STATUS_POSTC8000	98h	ROM C800h extension returned.
POST_STATUS_TIMERPRNBASE	99h	Configure timer/printer data.
POST_STATUS_SERIALBASE	9ah	Configure serial port base addresses.
POST_STATUS_INITBEFORENPX	9bh	Prepare to initialize coprocessor.
POST_STATUS_INITNPX	9ch	Initialize numeric coprocessor.
POST_STATUS_POSTNPX	9dh	Numeric coprocessor initialized.
POST_STATUS_CHECKLOCKS	9eh	Check KB settings.
POST_STATUS_ISSUEKBDID	9fh	Issue keyboard ID command.
POST_STATUS_RESETID	0a0h	KB ID flag reset.
POST_STATUS_TESTCACHE	0a1h	Test cache memory.
POST_STATUS_DISPSOFTERR	0a2h	Display soft errors.
POST_STATUS_TYPEMATIC	0a3h	Set keyboard typematic rate.
POST_STATUS_MEMWAIT	0a4h	Program memory wait states.
POST_STATUS_CLRSCR	0a5h	Clear screen.
POST_STATUS_ENABPTYNMI	0a6h	Enable parity and NMIs.

POST_STATUS_INITE000	0a7h	Initialize before calling ROM at E000h.
POST_STATUS_CALLE000	0a8h	Call ROM BIOS extension at E000h.
POST_STATUS_POSTE000	0a9h	ROM extension returned.
POST_STATUS_DISPCONFIG	0b0h	Display system configuration box.
POST_STATUS_INT19BOOT	00h	Call INT 19h bootstrap loader.
POST_STATUS_LOWMEMEXH	0b1h	Test low memory exhaustively.
POST_STATUS_EXTMEMEXH	0b2h	Test extended memory exhaustively.
POST_STATUS_PCIENUM	0b3h	Enumerate PCI busses.

6.9 Critical Error Beep Codes

Embedded BIOS tests much of the hardware early in POST before messages can be displayed on the screen. When system failures are encountered at these early stages, POST uses beep codes (a sequence of tones on the speaker) to identify the source of the error.

The following is a comprehensive list of POST beep codes for the system BIOS. BIOS extensions, such as VGA ROMs and SCSI adapter ROMs, may use their own beep codes, including short/long sequences, or possibly beep codes that sound like the ones below. When diagnosing a system failure, remove these adapters if possible before making a final determination of the actual POST test that failed.

Mnemonic Code	Beep Count	Description of Problem
POST_BEEP_REFRESH	1	Memory refresh is not working.
POST_BEEP_PARITY	2	Parity error found in 1st 64KB of memory.
POST_BEEP_BASE64KB	3	Memory test of 1st 64KB failed.
POST_BEEP_TIMER	4	T1 timer test failed.
POST_BEEP_CPU	5	CPU test failed.
POST_BEEP_GATEA20	6	Gate A20 test failed.
POST_BEEP_DMA	7	DMA page/base register test failed.
POST_BEEP_VIDEO	8	Video controller test failed.
POST_BEEP_KEYBOARD	9	Keyboard test failed.
POST_BEEP_SHUTDOWN	10	CMOS shutdown register test failed.
POST_BEEP_CACHE	11	External cache test failed.
POST_BEEP_BOARD	12	General board initialization failed.
POST_BEEP_LOWMEM	13	Exhaustive low memory test failed.
POST_BEEP_EXTMEM	14	Exhaustive extended memory test failed.
POST_BEEP_CMOS	15	CMOS restart byte test failed.
POST_BEEP_ADDRESS_LINE	16	Address line test failed.
POST_BEEP_DATA_LINE	17	Data line test failed.
POST_BEEP_INTERRUPT	18	Interrupt controller test failed.
POST_BEEP_PASSWORD	1	Incorrect password used to access SETUP.

P64H2 Riser Card 7

7.1 Introduction

The P64H2 Riser Card is an optional component of the Intel E7500 Scalable Performance Board Development Kit. The Intel RGE7500PL Memory Controller Hub (MCH) supports up to three HI 2.0 connections. The board contains two Intel P64H2 components connected via HI 2.0 expansion slot. The riser card enables you to use the third HI 2.0 to provide a third P64H2 on the board.

The P64H2 Riser Card consists of one P64H2 component and three 3.3V PCI-X connectors. Bus A contains one PCI-X connector running up to 133 MHz, and Bus B contains two connectors running up to 100 MHz. Figure 21 depicts the block diagram.

Figure 21. P64H2 Riser Card Block Diagram

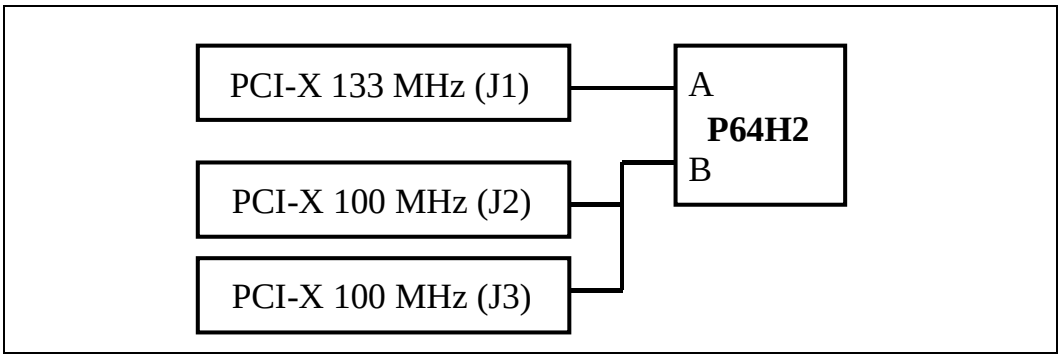
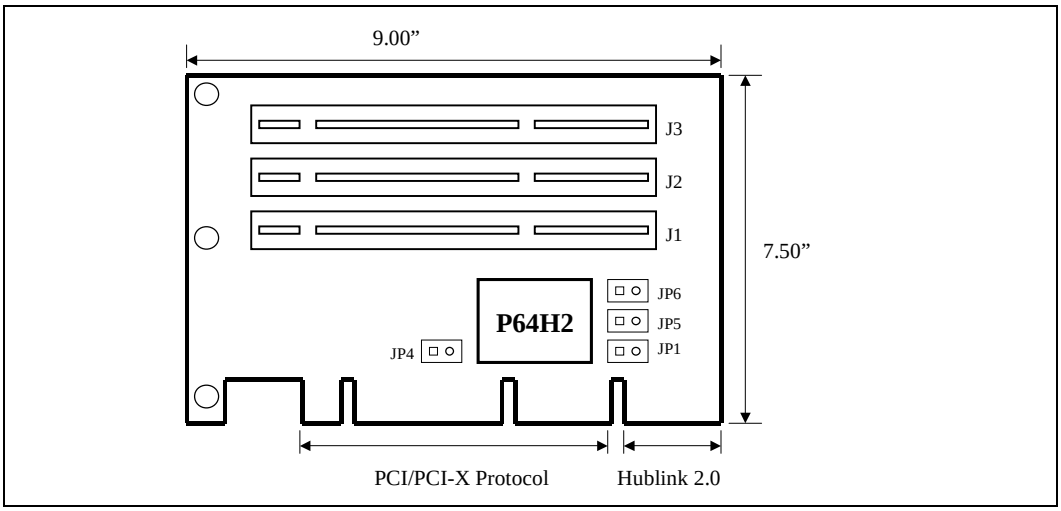


Figure 22 depicts the riser card's dimensions and the placement of the components on the board. The riser card measures 9.00" x 7.50". (Note: The figure is not drawn to scale.)

Figure 22. P64H2 Riser Card Topology

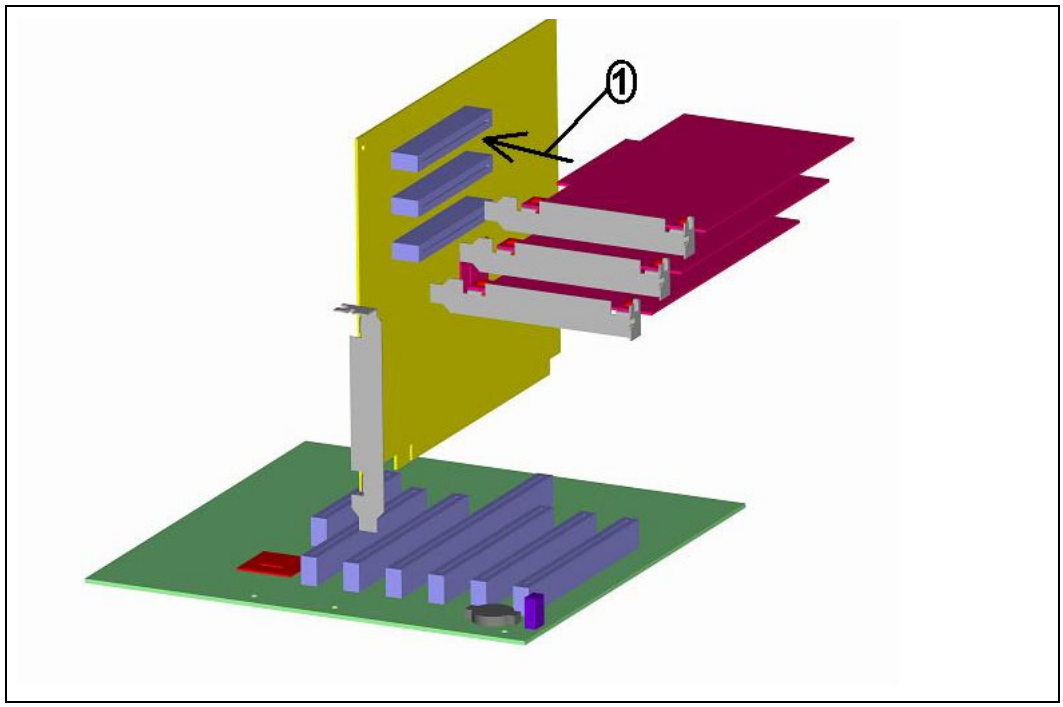


7.2 Hardware Installation

The P64H2 Riser Card hardware includes a steel bracket designed to support the weight of PCI/PCI-X cards connected to the riser card. Refer to Figure 7, “Board Layout Diagram” on page 38 and follow these steps to install the hardware:

1. Insert one, two or three PCI/PCI-X cards into the slots on the riser card. See Figure 23.

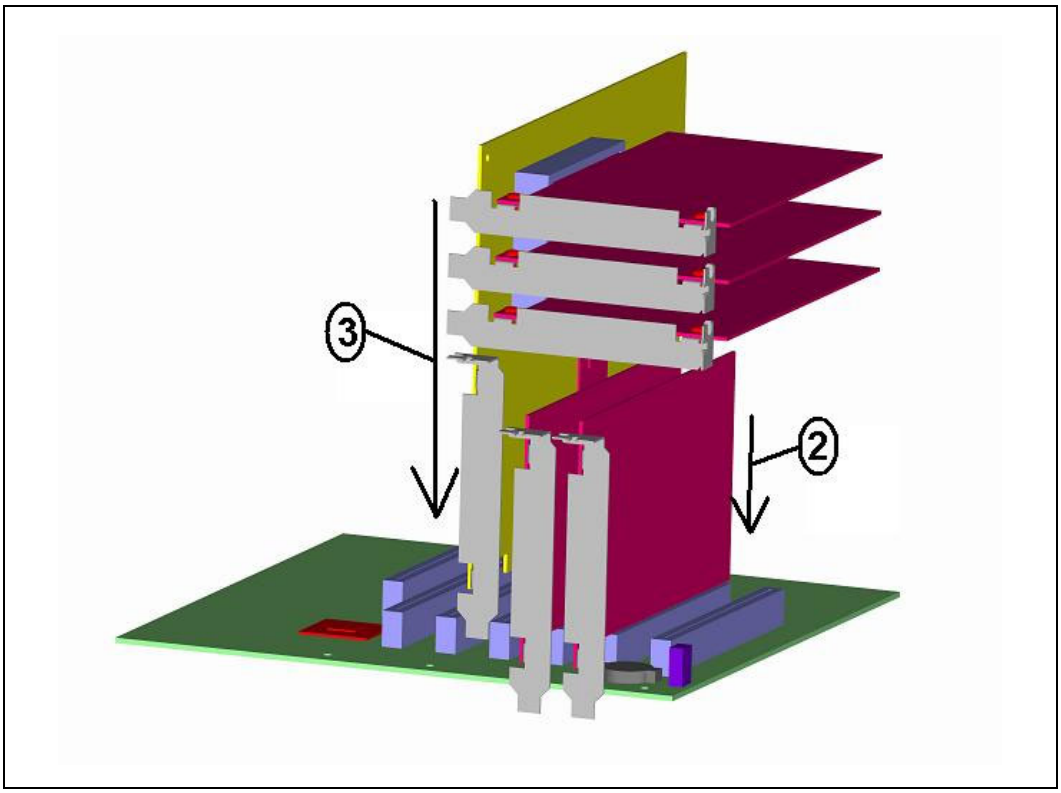
Figure 23. Inserting PCI/PCI-X Cards into the Slots on the Riser Card



2. If you are using slots J24 or J25 on the evaluation board, insert PCI/PCI-X cards into those slots before installing the P64H2 Riser Card, as shown in Figure 24. If you are using slot J23, ensure that this slot is empty until step 6 of this installation procedure.
3. Plug the P64H2 Riser Card into slot J12 of the evaluation board (the largest slot on the board). See Figure 24.

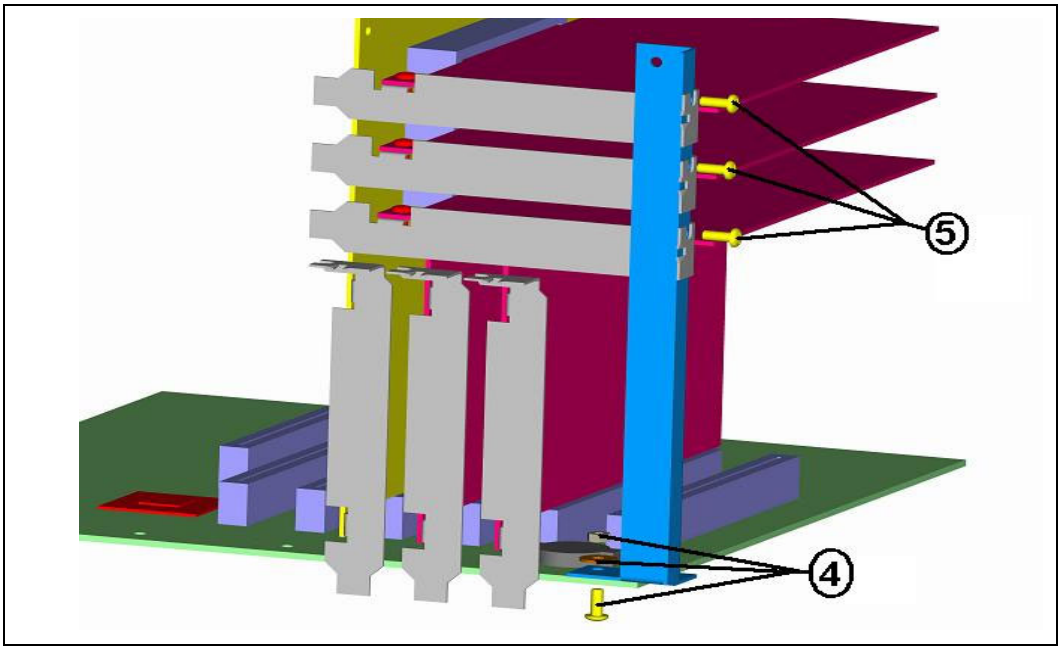
Note: Plug PCI/PCI-X cards into the evaluation board first, then plug in the Riser Card.

Figure 24. Installing the P64H2 Riser Card



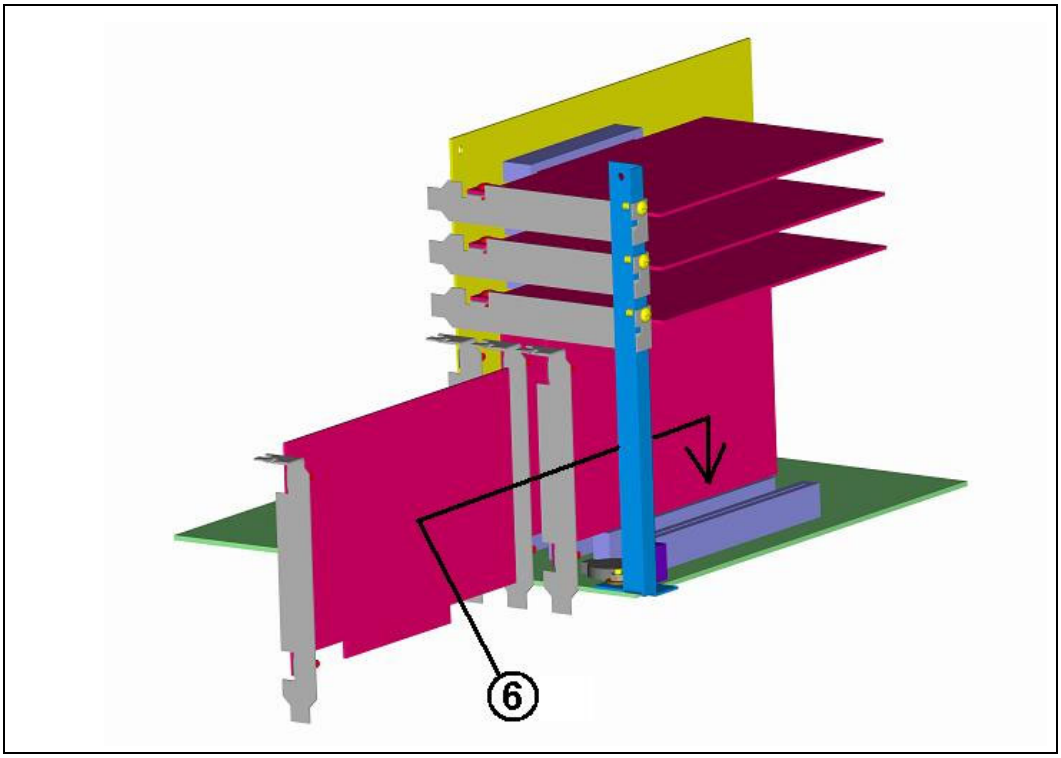
4. Install the P64H2 steel bracket by first attaching it to the evaluation board baseboard using (1) 6-32 x 3/8 screw, (1) 6-32 nut, and (1) 6-32 washer.
5. Attach the faceplates of the PCI cards to the bracket using (3) 6-32 x 3/8 screws as shown in Figure 25.

Figure 25. Installing the Bracket



6. If you are using slot J23, you can insert a PCI/PCI-X card by sliding it through the bracket enclosure and plugging it into the evaluation board. See Figure 26.

Figure 26. Inserting the PCI/PCI-X Card into Slot J23



7.3 Hardware Configuration

7.3.1 Jumper Settings

There are two sets of jumpers that control the speed of the PCI-X buses. Table 31 describes the jumper settings for Channel A (one 133 MHz slot), and Table 32 describes the jumper settings for Channel B (two 100 MHz slots).

Table 31. Channel A Jumper Settings

JP1	JP4	Protocol	Frequency
No Jumper	No Jumper	PCI-X	Default - 133 MHz
Jumper	No Jumper	PCI-X	100 MHz
Jumper	Jumper	Not a supported configuration	
No Jumper	Jumper	Not a supported configuration	

Table 32. Channel B Jumper Settings

JP5	JP6	Protocol	Frequency
No Jumper	Jumper	PCI-X	Default – 100 MHz
Jumper	No Jumper	PCI-X	133 MHz
Jumper	Jumper	Not a supported configuration	
No Jumper	No Jumper	Not a supported configuration	

7.3.2 Hot Plug and Bootable Devices

Hot plug and bootable devices are not supported on the P64H2 Riser Card.

Bill of Materials A

This appendix includes the latest bill of materials as of this printing. To obtain the latest version of the bill of materials, go to http://developer.intel.com/design/intarch.

Table 33. Bill of Materials (Sheet 1 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
1	BH1	BAT ACC,HOLDR,THM,CR2032	CHIA TSE TERMINAL INDUSTRY CO., LT	B7566BP5R
63	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C520, C521, C522, C523, C524, C680, C683, C684, C685, C688, C689, C692, C693, C700, C701, C1398, C1399, C1404, C1405, C1531, C1546, C1587, C1588	CAPC,X5R,1210,22.000 UF,6.300V,+/- 20%	TDK CORPORATION OF AMERICA	C3225X5R0J226MT009N
68	C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C65, C66, C67, C68, C303, C304, C335, C346, C456, C457, C458, C459, C527, C528, C882, C904, C1045, C1046, C1047, C1048, C1049, C1050, C1051, C1052, C1057, C1058, C1059, C1060, C1061, C1062, C1063, C1064, C1078, C1079, C1080, C1112, C1113, C1114, C1115, C1124, C1134, C1135, C1136, C1137, C1506, C1547, C1551, C1554, C1571, C1572, C1573, C1574	CAPC,X5R,0805,1.000 UF,16.000V,+/- 10%	MURATA ELEC. NORTH AMERICA	GRM40X7R105K016AK
24	C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C1475, C1476, C1477, C1478	CAPA,560.000 UF,8X11,4.000V,+/- 20%,TH	SANYO VIDEO COMPONENTS	4SP560M+C3

Table 33. Bill of Materials (Sheet 2 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
454	C289, C290, C291, C292, C293, C294, C295, C296, C297, C298, C299, C300, C301, C302, C305, C306, C307, C308, C309, C310, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C513, C515, C516, C517, C518, C615, C616, C646, C777, C780, C781, C783, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834, C835, C836, C837, C838, C839, C840, C841, C842, C843, C844, C845, C846, C847, C848, C849, C850, C851, C852, C853, C854, C855, C856, C857, C858, C859	CAPC,X7R,0603,0.100 UF,16.000V,+/- 10%	TDK CORPORATION OF AMERICA	C1608X7R1C104KT009T

Table 33. Bill of Materials (Sheet 3 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
40	C437, C438, C439, C440, C441, C442, C443, C444, C635, C642, C648, C649, C650, C651, C1272, C1273, C1274, C1279, C1281, C1282, C1283, C1284, C1285, C1286, C1287, C1288, C1290, C1301, C1302, C1303, C1339, C1340, C1449, C1560, C1575, C1576, C1602, C1603, C1604, C1605	CAPC,X7R,0603,1000.000 PF,50.000V,+/- 1>	TDK CORPORATION OF AMERICA	C1608X7R1H102KT009A
13	C445, C446, C447, C448, C449, C450, C897, C898, C899, C900, C901, C902, C903	CAPC,Y5V,1210,10.000 UF,16.000V,+80/-20>	TDK CORPORATION OF AMERICA	C3225Y5V1C106ZT0S9N
63	C451, C452, C453, C454, C713, C714, C715, C716, C717, C718, C719, C720, C721, C722, C723, C724, C725, C726, C727, C905, C906, C907, C908, C913, C914, C915, C916, C1041, C1042, C1053, C1054, C1081, C1085, C1086, C1089, C1090, C1091, C1093, C1094, C1095, C1096, C1097, C1098, C1099, C1100, C1101, C1106, C1107, C1108, C1110, C1111, C1125, C1126, C1129, C1130, C1131, C1132, C1133, C1548, C1549, C1550, C1552, C1553	CAPC,X7R,0805,0.100 UF,50.000V,+/- 20%	TDK CORPORATION OF AMERICA	C2012X7R1H104MT0S9N
1	C455	CAPC,C0G,0805,120.000 PF,50.000V,+/- 5%>	MURATA ELEC. NORTH AMERICA	GRM40C0G121J050AJ

Table 33. Bill of Materials (Sheet 4 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
131	C498, C511, C589, C590, C595, C596, C597, C598, C613, C614, C620, C621, C631, C638, C778, C779, C782, C784, C889, C1269, C1276, C1277, C1278, C1291, C1293, C1294, C1295, C1296, C1297, C1298, C1299, C1300, C1304, C1305, C1306, C1309, C1312, C1313, C1314, C1315, C1316, C1317, C1318, C1321, C1322, C1325, C1326, C1327, C1328, C1329, C1330, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1342, C1343, C1344, C1345, C1346, C1347, C1348, C1349, C1350, C1351, C1352, C1353, C1354, C1355, C1356, C1357, C1358, C1359, C1360, C1361, C1362, C1363, C1364, C1365, C1366, C1367, C1368, C1369, C1370, C1371, C1374, C1375, C1376, C1379, C1450, C1530, C1598, C1599, C1607, C1608, C1609, C1610, C1611, C1612, C1613, C1614, C1615, C1616, C1617, C1618, C1619, C1620, C1621, C1622, C1623, C1624, C1625, C1649, C1650, C1651, C1652, C1653, C1654, C1655, C1656, C1657, C1658, C1659, C1660, C1668, C1671, C1672	CAPC,X7R,0603,0.010 UF,50.000V,+/- 10%	MURATA ELEC. NORTH AMERICA	GRM39X7R103K050AJ
1	C512	CAPC,X7R,0603,2200.000 PF,50.000V,+/- 1>	TDK CORPORATION OF AMERICA	C1608X7R1H222KT009A
4	C702, C703, C704, C705	CAPC,X7R,0603,2200.000 PF,50.000V,+/- 1>	TDK CORPORATION OF AMERICA	C3216X7R0J106MT0S9N
8	C530, C531, C532, C533, C1555, C1556, C1557, C1558	CAPS,AL-P,E/X,180.000 uF,4.000V,+/- 20%>	PANASONIC INDUSTRIAL	EEFUE0G181R
16	C534, C535, C536, C537, C538, C539, C540, C541, C1261, C1262, C1263, C1264, C1265, C1266, C1267, C1268	CAPC,X7R,0603,220.000 PF,50.000V,+/- 10>	MURATA ELEC. NORTH AMERICA	GRM39X7R221K050AJ

Table 33. Bill of Materials (Sheet 5 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
18	C605, C606, C607, C608, C609, C610, C611, C612, C1065, C1066, C1067, C1068, C1069, C1070, C1074, C1075, C1076, C1077	CAPC,X7R,0805,0.033 UF,50.000V,+/- 10%	TDK CORPORATION OF AMERICA	C2012X7R1H333KT0J9N
3	C617, C1372, C1373	CAPC,X7R,0603,0.047 UF,16.000V,+/- 10%	TDK CORPORATION OF AMERICA	C1608X7R1C473KT009N
1	C618	CAPC,C0G,0603,15.000 PF,50.000V,+/- 5%	TDK CORPORATION OF AMERICA	C1608C0G1H150JT009A
1	C619	CAPC,C0G,0603,10.000 PF,50.000V,+/- 0.5>	TDK CORPORATION OF AMERICA	C1608C0G1H100DT009A
9	C622, C623, C624, C644, C1561, C1593, C1594, C1595, C1596	CAPC,C0G,0603,47.000 PF,50.000V,+/- 5%	TDK CORPORATION OF AMERICA	C1608C0G1H470JT009A
8	C628, C629, C1240, C1241, C1448, C1451, C1452, C1453	CAPC,C0G,0603,470.000 PF,50.000V,+/- 5%>	MURATA ELEC. NORTH AMERICA	GRM39C0G471J050AJ
10	C632, C633, C634, C639, C640, C641, C1505, C1559, C1562, C1565	CAPC,C0G,0603,100.000 PF,50.000V,+/- 5%>	MURATA ELEC. NORTH AMERICA	GRM39C0G101J050AJ
2	C645, C1563	CAPC,X7R,0603,330.000 PF,50.000V,+/- 10>	MURATA ELEC. NORTH AMERICA	GRM39X7R331K050AJ
2	C656, C657	CAPT,E,1000UF,4V,+/-20%	KEMET	T510E108M004AS
2	C658, C659	CAPT,E/X,330.000 UF,10.000V,+/- 20%	KEMET	T491X337M010AS7454
4	C664, C665, C666, C667	CAPT,E/X,33.000 UF,20.000V,+/- 20%,FUSE>	KEMET	T496X336M020AS7454
14	C681, C682, C686, C687, C690, C691, C694, C695, C1400, C1401, C1402, C1403, C1543, C1544	CAPT,D,22.000 UF,16.000V,+/- 20%,FUSED	KEMET	T496D226M016AS7454
32	C706, C709, C881, C1410, C1411, C1414, C1415, C1416, C1419, C1421, C1422, C1423, C1424, C1425, C1426, C1427, C1428, C1429, C1430, C1431, C1432, C1433, C1434, C1441, C1589, C1601, C1606, C1627, C1628, C1629, C1630, C1631	CAPT,B,10.000 UF,16.000V,+/- 20%	KEMET	T491B106M016AS7454
18	C710, C711, C1390, C1391, C1392, C1393, C1394, C1395, C1396, C1397, C1435, C1436, C1437, C1438, C1439, C1440, C1566, C1600	CAPT,A,4.70 uF,10.000V,+/- 20%	VISHAY- SPRAGUE	293D475X0010A2W

Table 33. Bill of Materials (Sheet 6 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
1	C712	CAPT,A,2.2UF,6V,+/-20%	KEMET	T491A225M006AS
24	C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C1567, C1568, C1569, C1570	CAPT,C,100UF,6V,+/-10%	KEMET	T491C107K006AS
1	C776	CAPT,C,22.000 UF,16.000V,+/-20%	AVX/KYOCERA	TAJC226M016R
8	C909, C910, C911, C912, C1043, C1044, C1055, C1056	CAPC,X7R,0805,0.010 UF,50.000V,+/- 10%	TDK CORPORATION OF AMERICA	C2012X7R1H103KT009N
2	C1127, C1128	CAPC,X7R,0805,0.470 UF,16.000V,+/- 10%	TDK CORPORATION OF AMERICA	C2012X7R1C474KT0S9N
2	C1243, C1564	CAPC,Y5V,0603,0.220 UF,16.000V,+80/-20%>	TDK CORPORATION OF AMERICA	C1608Y5V1C224ZT009N
17	C1244, C1245, C1246, C1247, C1248, C1249, C1250, C1251, C1252, C1253, C1254, C1255, C1256, C1257, C1258, C1259, C1260	CAPC,C0G,0603,180.000 PF,50.000V,+/- 5%>	MURATA ELEC. NORTH AMERICA	GRM39C0G181J050AJ
2	C1270, C1271	CAPC,C0G,0603,22.000 PF,50.000V,+/- 5%	TDK CORPORATION OF AMERICA	C1608C0G1H220JT009A
6	C1320, C1323, C1377, C1502, C1641, C1642	CAPC,X5R,0603,1.000 UF,6.300V,+/- 20%	TDK CORPORATION OF AMERICA	C1608X5R0J105MT009N
8	C1442, C1443, C1444, C1445, C1446, C1447, C1479, C1577	CAPA,270.000 UF,10X10,16.000V,+/- 20%,T>	SANYO VIDEO COMPONENTS	16SP270M+C3
4	C1481, C1482, C1483, C1484	CAPA,820.000 UF,10X11,4.000V,+/- 20%,TH>	SANYO VIDEO COMPONENTS	4SP820M+C3
6	C1496, C1497, C1498, C1499, C1643, C1644	CAPC,0805,0.1UF,16V,+/-20%	MURATA ELEC. NORTH AMERICA	LLL216R71C104MA01
3	C1590, C1591, C1592	CAPT,C,100UF,6V,+/-10%,LOWESR	KEMET	T495C107K006AS7
1	C1626	CAPC,X7R,0603,1500.000 PF,50.000V,+/- 1>	MURATA ELEC. NORTH AMERICA	GRM39X7R152K050AJ
6	CR1, CR2, CR72, CR75, CR76, CR77	IC,DS,DIO,SOT-23,GP	PHILIPS COMPONENTS	BAV70
5	CR3, CR5, CR6, CR78, CR80	IC,DS,DIO,SOT-23,SHTKY	CENTRAL SEMICONDUCTOR CORP	CMPSH-3
4	CR4, CR7, CR26, CR79	IC,DS,DIO,SMB,MBRS130T3,SHTKY	SEMICONDUCTOR COMPONENTS INDUSTRIE	MBRS130T3

Table 33. Bill of Materials (Sheet 7 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
4	CR37, CR38, CR39, CR40	IC,DS,DIO,SOT-23,SHTKY	I T T SEMICONDUCTOR	BAT54C
1	CR45	IC,DS,DIO,SOT-23,GP	SEMICONDUCTOR COMPONENTS INDUSTRIE	MMBD914LT1
2	CR46, CR47	IC,DS,DIO,D-PAK,MBRD320T4,SHTKY	SEMICONDUCTOR COMPONENTS INDUSTRIE	MBRD320T4
5	CR49, CR50, CR51, CR52, CR53	IC,DS,DIO,SOT-23,BAT54SL1,SHTKY	PHILIPS COMPONENTS	BAT54S
7	CR54, CR56, CR60, CR62, CR64, CR66, CR68	LED,SM,GRN,V,1,RC,1	STANLEY ELECTRIC SALES OF AMERICA	PG1112H-CR
7	CR55, CR57, CR61, CR63, CR65, CR67, CR81	LED,SM,AMBER,V,1,RC,1	STANLEY ELECTRIC SALES OF AMERICA	AA1112H-TR
1	CR74	DIO,SHTKY,BARR,RECT,.5AMP,20V	ON SEMICONDUCTOR	MBR0520LT1
6	FB1, FB2, FB3, FB27, FB28, FB29	FER-BEAD,0603,60.0 OHM,0.5 A,± 25%	MURATA ELEC. NORTH AMERICA	BLM11P600SPT1
2	FB4, FB5	FER-BEAD,0805,30.0 OHM,3.0 A,± 25%	MURATA ELEC. NORTH AMERICA	BLM21P300SPT1
7	FB6, FB7, FB8, FB9, FB10, FB30, FB31	FERRITE BEAD,SMD,70 MHZ	MURATA ELEC. NORTH AMERICA	BLM31A700SPT1
5	FB13, FB14, FB15, FB16, FB18	FER-BEAD,1206,50.0 OHM,3.0 A,± 25%	MURATA ELEC. NORTH AMERICA	BLM31P500SPT1
1	FB17	FER-BEAD,1206,120.0 OHM,0.2 A,± 25,AR	TDK CORPORATION OF AMERICA	ACA3216M4-120-TL
8	J2, J3, J4, J5, J6, J7, J8, J9	CONN,CEDG,184P,DIMM,VT,0.05,062ST	FCI	55635-23302
1	J10	CONN,I/O,8P,USB,RA,.09,093ST	FOXCONN ELECTRONICS, INC.	UB11123-5D1
1	J11	CONN,CEDG,120P,PCI,VT,0.05,093ST	FOXCONN ELECTRONICS, INC.	EH06011-PC-W
1	J12	CONN,MISC,254 P,PCI 093ST,IVXB METAL	FOXCONN ELECTRONICS, INC.	EH0C107-3B
1	J13	CONN,HDR,2 X 13,PLG,VT,2MM,SMT,KP 26	FCI	61698-302TR
1	J16	CONN,HDR,2 X 20,PLG,VT,0.1,062ST,KP 20,>	FOXCONN ELECTRONICS, INC.	HL09207-D2
2	J17, J18	CONN,SKT,604P,MPGA,0.05,SMT,ZIF	TYCO ELECTRONICS CORPORATION	1489691-1

Table 33. Bill of Materials (Sheet 8 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
2	J19, J36	CONN,HDR,2X5,PLG,VT,0.1,062ST,KP PG	MOLEX CONNECTOR CORPORATION	90367-7012
5	J20, J21, J23, J24, J25	CONN,CEDG,184P,PCI,VT,0.05,062ST	TYCO ELECTRONICS CORPORATION	145168-2
1	J27	CONN,HDR,1 X 4,PLG,VT,0.1,062ST,KP SHR >	TYCO ELECTRONICS CORPORATION	640456-4
1	J29	CONN,I/O,15P,DSUB,RA,0.05,062ST,SHIELDE>	FOXCONN ELECTRONICS, INC.	DZ11A36-R9
1	J31	CONN,I/O,25P,DSUB,RA,.109,093ST	FOXCONN ELECTRONICS, INC.	DM11356-R1
1	J34	CONN,HDR,2 X 17,PLG,VT,0.1,062ST,KP 5,S>	WIESON ELECTRONIC	2120C888-001
1	J35	CONN,I/O,9P,DSUB,RA,.109,062ST	FOXCONN ELECTRONICS, INC.	DT10126-R9
2	J37, J38	68PIN,SCSI-2,RECEPTACLE	METHODE ELECTRONICS INC	S2A-SR-68-3-BL-2
1	J39	CONN,I/O,8P,RJ45,RA,0.05,062ST,W/LEDS	TYCO ELECTRONICS CORPORATION	1116075-4
1	J40	CONN,I/O,12P,DIN,RA,0.1,093ST	FOXCONN ELECTRONICS, INC.	MH11061-D5-N
1	J43	CONN,HDR,2 X 15,PLG,VT,0.1,062ST,KP SHR>	FOXCONN ELECTRONICS, INC.	HL17156
1	J70	CONN,HDR,2 X 10,PLG,VT,0.1,062ST,KP SHR>	FOXCONN ELECTRONICS, INC.	HL17106
1	J71	HDR,2X15,SMT,0.100 PITCH	TYCO ELECTRONICS CORPORATION	1-146134-4
15	JP1, JP2, JP7, JP24, JP25, JP26, JP27, JP28, JP29, JP30, JP31, JP32, JP33, JP34, J42	CONN,HDR,1 X 2,PLG,VT,0.1,062ST,KP 0.23>	WIESON ELECTRONIC	2100C888-051
7	JP3, JP4, JP35, JP38, JP39, JP40, JP41	CONN,HDR,1 X 3,PLG,VT,0.1,062ST,KP 0.23>	WIESON ELECTRONIC	2100C888-001
4	L3, L4, L5, L6	INDCT,4.70 uH,30.000 mA,10.00%,0805	MURATA ELEC. NORTH AMERICA	LQG21N4R7K10T2
4	L7, L8, L12, L22	CHOKE,COIL,PWR,1.0OUH,	PANASONIC INDUSTRIAL INC.	ETQP6F1R2HFA
4	L13, L14, L15, L16	INDCT,450.00 nH,15.00 A,25.00%,0.00400O>	BI TECHNOLOGIES	HM00-99696

Table 33. Bill of Materials (Sheet 9 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
1	L17	INDCT,1.90 uH,18.00 A,20.00%,0.00500OHM>	BI TECHNOLOGIES	HM00-99522
1	L18	IND,1.5UH,13.4MA,+/-20.00%	COILTRONICS	UP4B-1R5
1	L19	INDCT,54.00 nH,920.000 mA,10.00%,1206	MURATA ELECT. NORTH AMERICA	LQH31HN54NK01L
2	L20, L21	INDCT,0.10 uH,250.000 mA,10.00%,0805	MURATA ELEC. NORTH AMERICA	LQG21NR10K10T2
12	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q49, Q50	IC,DS,FET N,SO8,FDS6670A	FAIRCHILD SEMICONDUCTOR CORP.	FDS6670A
12	Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q37, Q38, Q39, Q40	IC,DS,FET N,SO8,SI4410	SILICONIX	SI4410DY-T1-REVA
1	Q20	IC,DS,FET N,SOT-23,1NO2E	SEMICONDUCTOR COMPONENTS INDUSTRIE	MGSF1N02ELT
8	Q22, Q23, Q25, Q27, Q56, Q57, Q58, Q59	LGC,TO-220,80A,30V	FAIRCHILD SEMICONDUCTOR CORP	FDP6670AL
8	Q24, Q26, Q28, Q29, Q61, Q62, Q63, Q64	LGC,TO-220,100A,30V	FAIRCHILD SEMICONDUCTOR CORP	FDP7045L
5	Q32, Q33, Q53, Q60, Q65	IC,DS,NPN XSTR,SOT6,MBT3904	SEMICONDUCTOR COMPONENTS INDUSTRIE	MBT3904DW1T1
4	Q41, Q48, Q66, Q67	IC,DS,NPN XSTR,SOT-23	PHILIPS COMPONENTS	PMBT3904
2	Q43, Q44	SOIC,8P,10A,30V	FAIRCHILD SEMICONDUCTOR CORP	FDS6690S
2	Q54, Q55	IC,DS,FET N,SOT-23,BSS138	FAIRCHILD SEMICONDUCTOR CORP	BSS138
29	R1, R2, R5, R6, R30, R34, R58, R62, R65, R67, R69, R97, R545, R546, R547, R548, R549, R550, R665, R666, R667, R668, R669, R670, R671, R672, R753, R754, R1025	RES D,0603,49.900OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#49R9

Table 33. Bill of Materials (Sheet 10 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
82	R12, R41, R42, R296, R298, R299, R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R310, R311, R314, R315, R316, R317, R318, R333, R340, R346, R352, R379, R380, R383, R466, R467, R483, R491, R497, R520, R531, R532, R559, R562, R569, R570, R571, R573, R629, R630, R631, R632, R633, R646, R652, R659, R662, R688, R689, R700, R709, R760, R761, R773, R774, R798, R799, R800, R832, R835, R900, R908, R909, R910, R922, R936, R937, R938, R948, R960, R995, R1019, R1037, R1040, R1047, R1049	RES D,0603,1000.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#102
4	R8, R10, R510, R2010	RES D,0603,56.00 OHM,5.00%,1/16W	AVX CERAMICS CORP	CR10-560J-K
2	R11, R939	RES D,0603,680.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#681
17	R16, R273, R279, R331, R338, R344, R350, R404, R430, R472, R488, R651, R679, R740, R759, R1020, R1036	RES D,0603,100.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#101
7	R28, R492, R512, R661, R663, R830, R831	RES D,0603,300.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#301
32	R7, R22, R23, R24, R25, R26, R27, R29, R35, R46, R47, R48, R49, R50, R51, R52, R53, R55, R56, R57, R77, R78, R79, R80, R81, R87, R1012, R1013, R1023, R1024, R1027, R1028	RES D,0603,51.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#510

Table 33. Bill of Materials (Sheet 11 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
65	R240, R353, R354, R355, R368, R371, R375, R378, R381, R382, R385, R386, R389, R405, R422, R431, R468, R469, R470, R482, R489, R530, R534, R535, R538, R539, R576, R604, R606, R608, R613, R614, R617, R649, R714, R747, R752, R765, R766, R790, R793, R794, R803, R804, R805, R806, R807, R808, R809, R812, R934, R940, R1021, R1022, R1029, R1030, R1031, R1035, R1038, R1039, R1044, R1045, R1046, R1050, R1051	RES D,0603,10000.000OHM,5.00%, 1/16W	ROHM CORPORATION	MCR03EZ$J#103
61	R59, R60, R63, R89, R96, R117, R118, R123, R124, R125, R126, R134, R135, R147, R149, R156, R158, R161, R162, R164, R174, R175, R183, R184, R192, R193, R198, R433, R434, R435, R436, R458, R478, R519, R673, R674, R675, R676, R680, R768, R770, R771, R815, R840, R842, R920, R923, R924, R925, R926, R927, R928, R929, R956, R957, R963, R976, R2001, R2002, R2003, R2004	RES D,0603,0.00 OHM,5.00%,1/16W	PANASONIC INDUSTRIAL COMPANY	ERJ3GSY0R00A
5	R61, R64, R66, R68, R98	RES D,0603,100.000OHM,1.00%,1/ 16W	ROHM CORPORATION	MCR03EZ$F#1000
9	R70, R71, R72, R73, R74, R75, R76, R838, R1026	RES D,0603,200.000OHM,5.00%,1/ 16W	ROHM CORPORATION	MCR03EZ$J#201
4	R83, R93, R94, R84	RES D,0603,150.000OHM,1.00%,1/ 16W	ROHM CORPORATION	MCR03EZ$F#1500
4	R86, R461, R462, R463	RES D,0603,75.000OHM,1.00%,1/ 16W	ROHM CORPORATION	MCR03EZ$F#75R0
1	R85	RES D,0603,1500.000OHM,5.00%,1 /16W	ROHM CORPORATION	MCR03EZ$J#152

Table 33. Bill of Materials (Sheet 12 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
1	R88	RES D,0603,27.40 OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#27R4
6	R90, R91, R100, R105, R107, R111	RES D,0603,24.90 OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#24R9
2	R92, R95	RES D,0603,301.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#3010
4	R99, R106, R110, R112	RES D,0603,453.00 OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZHF4530
4	R101, R103, R108, R113	RES D,0603,499.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#4990
4	R102, R104, R109, R114	RES D,0603,392.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#3920
2	R115, R120	RES D,0603,6.98 OHM,1.00%,1/16W	VISHAY- DALE ELECTRONICS INC	CRCW06036R98FRT5
73	R128, R129, R133, R137, R138, R142, R143, R145, R151, R152, R154, R159, R165, R167, R169, R171, R173, R178, R180, R181, R188, R189, R191, R197, R200, R201, R205, R206, R211, R216, R218, R219, R225, R227, R228, R233, R236, R241, R243, R262, R263, R264, R265, R268, R269, R359, R360, R362, R565, R568, R572, R574, R578, R580, R581, R582, R609, R610, R611, R612, R932, R933, R975, R977, R978, R1005, R1006, R1041, R1042, R1043, R1053, R1054, R1055	RES D,0603,8200.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#822
1	R356	RES D,0603,78.70 OHM,1.00%,1/16W	PANASONIC INDUSTRIAL	ERJ3EKF78R7A
4	R232, R257, R357, R361	RES D,0603,261.00 OHM,1.00%,1/16W	VISHAY- DALE ELECTRONICS INC	CRCW06032610FRT5
2	R210, R260	RES D,0603,750.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#7500
14	R270, R275, R605, R615, R965, R966, R967, R968, R969, R970, R971, R972, R973, R974	RES D,0603,5600.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#562

Table 33. Bill of Materials (Sheet 13 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
16	R288, R289, R290, R291, R292, R293, R294, R295, R598, R599, R602, R603, R648, R735, R935, R1034	RES D,0603,330.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#331
4	R319, R325, R529, R591	RES D,0603,6040.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#6041
12	R320, R321, R322, R323, R324, R326, R327, R328,	RES D,2010,5.00 mOHM,1.00%,1/2W	VISHAY- DALE ELECTRONICS INC	WSL2010R005FR86
7	R332, R339, R345, R702, R708, R1016, R1017	RES D,0603,20000.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#203
3	R429, R455, R813	RES D,0603,1000000.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#105
36	R369, R384, R390, R471, R475, R485, R486, R487, R490, R494, R495, R496, R499, R682, R683, R697, R704, R757, R758, R772, R775, R776, R777, R778, R779, R780, R781, R782, R788, R789, R1011, R1018, R1032, R1033, R2000, R2011	RES D,0603,4700.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#472
1	R374	RES D,0603,18.20 OHM,1.00%,1/16W	ROHM CORPORATION	MCR03FZHF18R2
2	R376, R377	RES D,0603,10000000.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#106
29	R387, R397, R540, R541, R542, R543, R544, R553, R586, R587, R588, R589, R755, R756, R949, R951, R952, R953, R954, R955, R959, R996, R997, R998, R999, R1000, R1001, R1002, R1003	RES D,0603,33.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#330
2	R392, R395	RES D,0603,68000.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#683
4	R393, R394, R459, R816	RES D,0603,33000.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#333
6	R398, R399, R400, R401, R607, R616	RES D,0603,2200.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#222

Table 33. Bill of Materials (Sheet 14 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
3	R421, R460, R817	RES D,0603,10.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#100
1	R423	RES D,0603,17400.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#1742
1	R424	RES D,0603,8060.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#8061
2	R425, R426	RES D,2512,2.00 mOHM,5.00%,1W,METFLM	VISHAY-DALE	WSL2512R002JR86
3	R452, R693, R694	RES D,0603,1000.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#1001
2	R453, R819	RES D,0603,806.00 OHM,1.00%,1/16W	VISHAY-DALE	CRCW06038060FRT5
1	R457	RES D,2512,5.00 mOHM,5.00%,1W,METFLM	VISHAY-DALE	WSL2512R005JR86
1	R473	RES D,0603,510.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#511
3	R474, R763, R764	RES D,0603,1.00 OHM,5.00%,1/16W	KOA SPEER ELECTRONICS	RM73B1JTDD1R0J
1	R476	RES D,0603,2610.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#2611
1	R477	RES D,0603,121000.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#1213
1	R479	RES D,0603,15000.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#153
1	R480	RES D,0603,392000.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#3923
9	R484, R493, R509, R511, R824, R828, R913, R1048, R2012	RES D,0603,470.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#471
8	R500, R501, R502, R503, R504, R505, R506, R507	RES D,0805,330.000OHM,5.00%,1/10W	ROHM CORPORATION	MCR10&ZH$J*331
4	R521, R522, R525, R528	RES D,0603,13000.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#1302
4	R523, R524, R526, R527	RES D,0603,6.98 kOHM,1.00%,1/16W	PANASONIC INDUSTRIAL	ERJ3EKF6981A
1	R536	RES D,0603,475.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#4750

Table 33. Bill of Materials (Sheet 15 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
7	R551, R552, R899, R2006, R2007, R2008, R2009	RES D,0603,22.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#220
4	R560, R678, R600, R601	RES D,0603,2700.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#272
5	R653, R711, R713, R801, R802	RES D,0603,100000.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#104
1	R658	RES D,0603,2490.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#249
1	R660	RES D,0603,34.80 OHM,1.00%,1/16W	VISHAY- DALE ELECTRONICS	CRCW060334R8FRT5
1	R664	RES D,0603,53.600OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#53R6
1	R681	RES D,0603,6190.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#6191
1	R692	RES D,0603,1.05K,1%	VISHAY COMPONENTS	CRCW06031051FT
1	R695	RES D,0603,487.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#4870
2	R748, R749	RES D,0603,10000.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#1002
2	R750, R751	RES D,0603,4.70 OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZH$J#4R7
1	R814	RES D,2010,10.00 mOHM,1.00%,1/2W	VISHAY- DALE ELECTRONICS	WSL2010R010FR86
1	R818	RES D,0603,402.00 OHM,1.00%,1/16W	PANASONIC INDUSTRIAL	ERJ3EKF4020A
4	R820, R821, R822, R823	RES D,0603,4300.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#432
2	R841, R843	RES D,0603,47.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#470
2	R209, R259	RES D,0603,332.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#3320
6	R881, R882, R886, R887, R890, R891	RES D,0603,3300.000OHM,5.00%,1/16W	MCR03EZ$J#332	ROHM CORPORATION
6	R883, R884, R885, R888, R889, R892	RES D,0603,6200.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#622

Table 33. Bill of Materials (Sheet 16 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
5	R894, R895, R896, R897, R898	RES D,0603,43.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#430
2	R1007, R1008	RES D,0603,10200.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#1022
2	R1009, R1010	RES D,0603,7150.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#7151
1	R1014	RES D,0603,1960.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#1961
1	R1015	RES D,0603,340000.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#3403
46	RP13, RP14, RP15, RP16, RP17, RP18, RP19, RP20,RP21, RP22, RP23, RP24, RP25, RP26, RP27, RP28, RP29, RP30, RP31, RP32, RP33, RP34, RP35, RP66,RP67, RP68, RP69, RP70, RP71, RP72, RP73, RP74, RP75, RP76, RP77, RP78, RP79, RP80, RP81, RP82,RP83, RP84, RP85, RP86, RP87, RP88	RES A,1206,10.00 OHM,5.00%,1/4W,RPAK,4,>	KOA SPEER ELECTRONICS	CNK1J4TDD100J
3	RP119, RP144, RP204	RES A,1206,5.60 kOHM,5.00%,1/4W,RPAK-SM>	ROHM CORPORATION	MNR14$OABJ562
71	RP120, RP121, RP122, RP123, RP124, RP125, RP126, RP127, RP128, RP129, RP130, RP131, RP132, RP133, RP134, RP135, RP136, RP137, RP138, RP139, RP140, RP141, RP142, RP145, RP146, RP147, RP148, RP149, RP150, RP151, RP152, RP153, RP154, RP155, RP156, RP157, RP158, RP159, RP160, RP161, RP162, RP163, RP164, RP165, RP166, RP167, RP168, RP169, RP170, RP171, RP172, RP173, RP174, RP175, RP176, RP177, RP178, RP179, RP180, RP181, RP182,RP183,RP184, RP185, RP186, RP198, RP199, RP200, RP201, RP202, RP203	RES A,1206,8.20 kOHM,5.00%,1/4W,RPAK-SM>	KOA SPEER ELECTRONICS	CNK1J4TDD822J

Table 33. Bill of Materials (Sheet 17 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
3	RP191, RP197, RP274	RES A,1206,10.00 kOHM,5.00%,1/4W,RPAK-S>	ROHM CORPORATION	MNR14$OABJ103
1	RP196	RES A,1206,15.00 kOHM,5.00%,1/4W,RPAK-S>	ROHM CORPORATION	MNR14$0ABJ153
2	RP205, RP282	RES A,1206,1.00 kOHM,5.00%,1/4W,RPAK-SM>	ROHM CORPORATION	MNR14$OABJ102
6	RP206, RP208, RP211, RP212, RP283, RP190	RES A,1206,2.70 kOHM,5.00%,1/4W,RPAK-SM>	ROHM CORPORATION	MNR14$OABJ272
3	RP207, RP209, RP210	RES A,1206,33.00 OHM,5.00%,1/4W,RPAK-SM>	KOA SPEER ELECTRONICS	CNK1J4TDD330J
60	RP213, RP214, RP215, RP216, RP217, RP218, RP219,RP220, RP221, RP222, RP223, RP224, RP225, RP226,RP227, RP228, RP229, RP230, RP231, RP232, RP233,RP234, RP235, RP236, RP237, RP238, RP239, RP240,RP241, RP242, RP243, RP244, RP245, RP246, RP247,RP248, RP249, RP250, RP251, RP252, RP253, RP254,RP255, RP256, RP257, RP258, RP259, RP260, RP261,RP262, RP263, RP264, RP265, RP266, RP267, RP268,RP269, RP270, RP271, RP272	RES A,1206,22.000OHM 5.00%,1/4W,RPAK-SM>	KOA SPEER ELECTRONICS	CNK1J4TDD220J
1	RP273	RES A,1206,0.00 OHM,5.00%,1/4W,RPAK,4,8>	ROHM CORPORATION	MNR14E0ABJ000
1	RP276	RES A,1206,100.000OHM 5.00%,1/4W,RPAK-S>	ROHM CORPORATION	MNR14$OABJ101
1	RP277	RES A,1206,680.00 OHM,5.00%,1/4W,RPAK-S>	KOA SPEER ELECTRONICS	CNK1J4TDD681J
1	RP279	RES A,1206,75.000OHM 5.00%,1/4W,RPAK-SM>	ROHM CORPORATION	MNR14$OABJ750
3	RP280, RP288, RP289	RES A,1206,4.70 kOHM,5.00%,1/4W,RPAK-SM>	ROHM CORPORATION	MNR14$OABJ472
2	RT1, RT2	POLYSWITCH,SMT,2.600A	LITTELFUSE INC	1812L260MR
2	RT3, RT4	POLYSWITCH,SMT,2.000A	RAYCHEM CORPORATION	SMD200-2
1	RT5	POLYSWITCH,SMT,1.100A	RAYCHEM CORPORATION	MINISMDC110-2
2	S8, S9	CONN,SWIT,TACTILE,VT,SPST,2,50.0 mA,SMT>	E-SWITCH	TL3304AF160QJ
1	SP1	AUDIO XDCR,80OHM,2400HZ,85DB,THM,5V	CHALLENGE ELECTRONICS	DBX-05A

Table 33. Bill of Materials (Sheet 18 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
1	U1	IC,LIN,SSOP,LTC1929-PG,SWITCHING	LINEAR TECHNOLOGY	LTC1929CG-PG
2	U14, U15	ASSY,IC,CHIPSETS,RG,N/A,82870P2,A,2,QC2>	INTEL CORP	RG82870P2 QC28
4	U16, U127, U128, U129	IC,LOG,Q-SWITCH,TSSOP,SN74CBTL	TEXAS INSTRUMENTS	74CBTLV3125D
1	U18	IC,LIN,SOT23,LT1761ES5-1,VREG	LINEAR TECHNOLOGY	LT1761ES5-1.8
3	U19, U20, U74	IC,LIN,SSOP,HIP1011D,VREG	INTERSIL CORPORATION	HIP1011DCA-T
1	U21	IC,CPLD,CMOS PROG,ULTRAL37000	CYPRESS SEMICONDUCTOR CORP.	CY37128VP 100 125BBC
5	U22, U23, U24, U25, U80	IC,LOG,Q-SWITCH,TSSOP,6810,BUS	PERICOM SEMICONDUCTOR	PI5C6800CLX
20	U28, U29, U30, U31, U32, U33, U34, U35, U36, U37,U38, U39, U40, U41, U42, U43, U85, U86, U87, U88	IC,LOG,Q-SWITCH,TSSOP,PI5C16215CA,BUS	PERICOM SEMICONDUCTOR	PI5C16215CAX
2	U44, U115	IC,RGLTR,SW,LTC1735CS-1,SO16	LINEAR TECHNOLOGY CORP.	LTC1735CS-1
1	U45	ASSY,IC,CHIPSETS,FW,N/A,82801CA,B,2,360>	INTEL CORP	FW82801CA QC43
4	U48, U49, U50, U51	IC,LIN,SOIC,HIP6601,CNTRLR	INTERSIL CORPORATION	HIP6601ACB
4	U52, U53, U57, U77	IC,LOG, GATES,SOIC,74LVC00,NAND	TEXAS INSTRUMENT	SN74LVC00ADR
1	U54	IC,VLSI,VIDEO,M69000,BGA,256	ASILIANT TECHNOLOGIES	M69000
1	U55	IC,LIN,SOIC,HIP6311ACB-,VREG	INTERSIL INC	HIP6311ACB-T
1	U56	IC,VLSI,SIO,LPC47B272,QFP,100	STANDARD MICROSYSTEMS CORP	LPC47B272QFP
1	U58	IC,LOG,DIG-COMP,SOP,SN74HC682DW,MAGNITU>	TEXAS INSTRUMENT	SN74HC682DWR
1	U59	IC,PWR,TRPL SPLY,LT1326CMS8	LINEAR TECHNOLOGY CORP.	LT1326CMS8
1	U60	IC,CLK_GEN,56,SSOP,GNRTR	INTEGRATED CIRCUIT SYSTEMS	ICS932S203AF
1	U61	IC,LIN,INTF,RS232,GD75232,SSOP,RS232,0.>	TEXAS INSTRUMENT	GD75232DBR
1	U64	SEEPROM,S08 150W,93C66,3,3V	ATMEL	AT93C66-10SC-2.7

Table 33. Bill of Materials (Sheet 19 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
1	U65	XFMR LAN,1000 BASE T,SMT,24 Pins,SINGLE	BEL FUSE INC	S558-5999-P3
1	U66	ASSY,IC,CHIPSETS,RG,N/A,82861,A,3,QC47	INTEL CORP	RG82861 QC47
2	U67, U68	IC,LOG, BUFFER/DRIVER,SOIC,74LVT125	PHILIPS COMPONENTS	74LVT125D-T
2	U70, U71	IC,LIN,SOT23,TLV431A,VREF	TEXAS INSTRUMENT	TLV431ACDBVR
1	U72	IC,LOG, GATES,SOIC,74LVC14,INV	PHILIPS COMPONENTS	74LVC14AD-T
1	U76	OSC,XTAL,SMT,50-200MHZ,3.4VDC	NEL FREQUENCY CONTROLS	SJ-A2920-80.000M
1	U78	IC,VLSI,SCSI,AIC7902W,BGA,456	ADAPTEC	754113
1	U79	IC,ASIC,CORDOVA,A4,416 BGA	MARVELL TECHNOLOGY GROUP LTD.	88EC001-BAJ-P103
1	U82	IC,LOG, GATES,SOIC,SN74LVC08,AND	PHILIPS COMPONENTS	74LVC08AD-T
1	U83	IC,VREG,80-220	LINEAR TECHNOLOGY CORP.	LT1764ET
1	U84	IC,LIN RGLTR,LT1118CS8	LINEAR TECHNOLOGY CORP.	LT1118CS8
6	U93, U94, U95, U96, U97, U98	IC,LIN,TERM,TSSOP,DS2119M,SCSI	MAXIM	DS2119ME T&R
1	U99	IC,COMPARATOR,QUAD,LOW VOLT,	TEXAS INSTRUMENTS	LMV339
1	U101	IC,EEPROM,SOIC,10.000 NS,64X16	ATMEL	AT93C46-10SC-2.7
1	U103	IC,AMPL,DUAL,LOW PWR,	NATIONAL SEMICONDUCTOR	LM2904
1	U104	IC,FAN,80KHZ-1MHZ,20P,SOIC	FAIRCHILD SEMICONDUCTOR	FAN5066
1	U113	IC,LOG, GATES,SSOP,SN74ACT04DR,INV	TEXAS INSTRUMENT	SN74ACT04DR
1	U119	IC,LIN,DDPAK,LT1587,VREG	LINEAR TECHNOLOGY	LT1587CM
1	U120	SW,SGL FET,LVL SHF	TEXAS INSTRUMENTS	SN74CBTD1G125DBVR
4	U121, U122, U123, U124	SW,BUS,LVL SHF,DUAL FET	TEXAS INSTRUMENTS	SN74CBTD3306D
1	U125	IC,LOG,MULTIPLEX,SOIC,74HC4052,NI	SEMICONDUCTOR COMPONENTS INDUSTRIE	MC74HC4052DR2

Table 33. Bill of Materials (Sheet 20 of 20)

Quantity	Reference Description	Description	Manufacturer	Manufacturer P/N
1	U126	IC,LOG,FF/ LATCH,SOIC,74AHC74,D-F/F	TEXAS INSTRUMENT	SN74AHC74DR
1	Y1	XTAL,MOLD,32.7680,KHZ,0.002%,SM	RALTRON	619601-001
1	Y2	XTAL,HC49S,14.3182,MHZ,20,PF,0.005%,SM	RALTRON	630770-003
1	Y3	XTAL,HC49S,25.0000,MHZ,20,PF,0.005%,SM	RALTRON	630770-011
1	U69	CONN,SKT,32P,PLCC,0.05,SMT	TYCO ELECTRONICS CORPORATION	822475-1
1	B1	BAT,CELL,3.0V,200MAH,LI	MAXELL CORPORATION OF AMERICA	CR2032
1		CONN,MISC,2 P,HEADER,ANCHOR HOO	FOXCONN ELECTRONICS, INC	HB96030-K
2	R208, R258	RES D,0603,61.900OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#61R9
1	R358	RES D,0603,825.000OHM,1.00%,1/16W	ROHM CORPORATION	MCR03EZ$F#8250
1		ASSY,LBL,S/N,MARBLE CANYON	BRADY CORPORATION	THT-40-497-10
1	J100	CONN,HDR,VERT,DUAL,2X24,	MOLEX INC.	39-28-1243
1	J101	CONN,HDR,VERT,DUAL,2X22,	MOLEX INC.	39-28-1223
1	J102	CONN,HDR,VERT,DUAL,2X8, MINI	MOLEX INC.	39-29-9082
2	R2013, R2014	RES D,0603,220.000OHM,5.00%,1/16W	ROHM CORPORATION	MCR03EZ$J#221
1	Q68	IC,DS,PNP XSTR,SOT223,PZT751T1	SEMICONDUCTOR COMPONENTS INDUSTRIE	PZT751T1
11	J50, J51, J52, J53, J54, J55, J56, J57, J58, J59, J60	CONN,CEDG,60P,PCI,VT,0.05,062ST	TYCO ELECTRONICS CORPORATION	650090-6

Schematics B

Schematics are provided for the following items listed below. Schematics are available from the Intel Developer's web site at http://developer.intel.com/design/intarch.

- System Block Diagram
- Processor Connector 0
- Processor Connector 1
- Processor Decoupling
- ITP, CPU GTL VREF
- MCH System Bus
- MCH HUB I/F
- MCH Power/Ground
- DDR A Series Resistors
- DDR A DIMMs
- DDR A Term
- DDR B Series Resistors
- DDR B DIMMs
- DDR B Term
- P64H2 #1
- P64H2 #2
- P64H2 #1 PCI Pullups
- P64H2 #2 PCI Pullups
- PCI-X Slots hot plug logic
- PCI-X Slots power control
- Slots A-D hot plug logic
- PCI-X slots power control
- Slots A-D hot plug bus switches
- PCI-X slots 1, 2, A, B, C
- 82808AA - PCI-X Slot D
- ICH3
- ICH3, USB, IDE connectors
- 32-bit PCI slot (debug)
- Video
- Power connectors, VID/VRD control logic

- Voltage regulators, reset control
- CK-408B
- FWH, LPC connector (debug)
- SIO, Legacy I/O
- LAN
- SCSI
- Front panel connector, BMC connector
- SMBus mux logic
- Spare gates, mounting holes

DP Intel® Xeon™ Processor/Low Voltage Intel® Xeon™ Processor/ Intel® E7500 Chipset Evaluation Kit Board Schematics

Rev A2

THESE SCHEMATICS ARE SUBJECT TO CHANGE.

TITLE:			Rev: A2
intel	EID Chandler, Arizona	DRAWN BY: TCL LAST REVISED: 8/08/02	PROJECT: MC 1 OF 83

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TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
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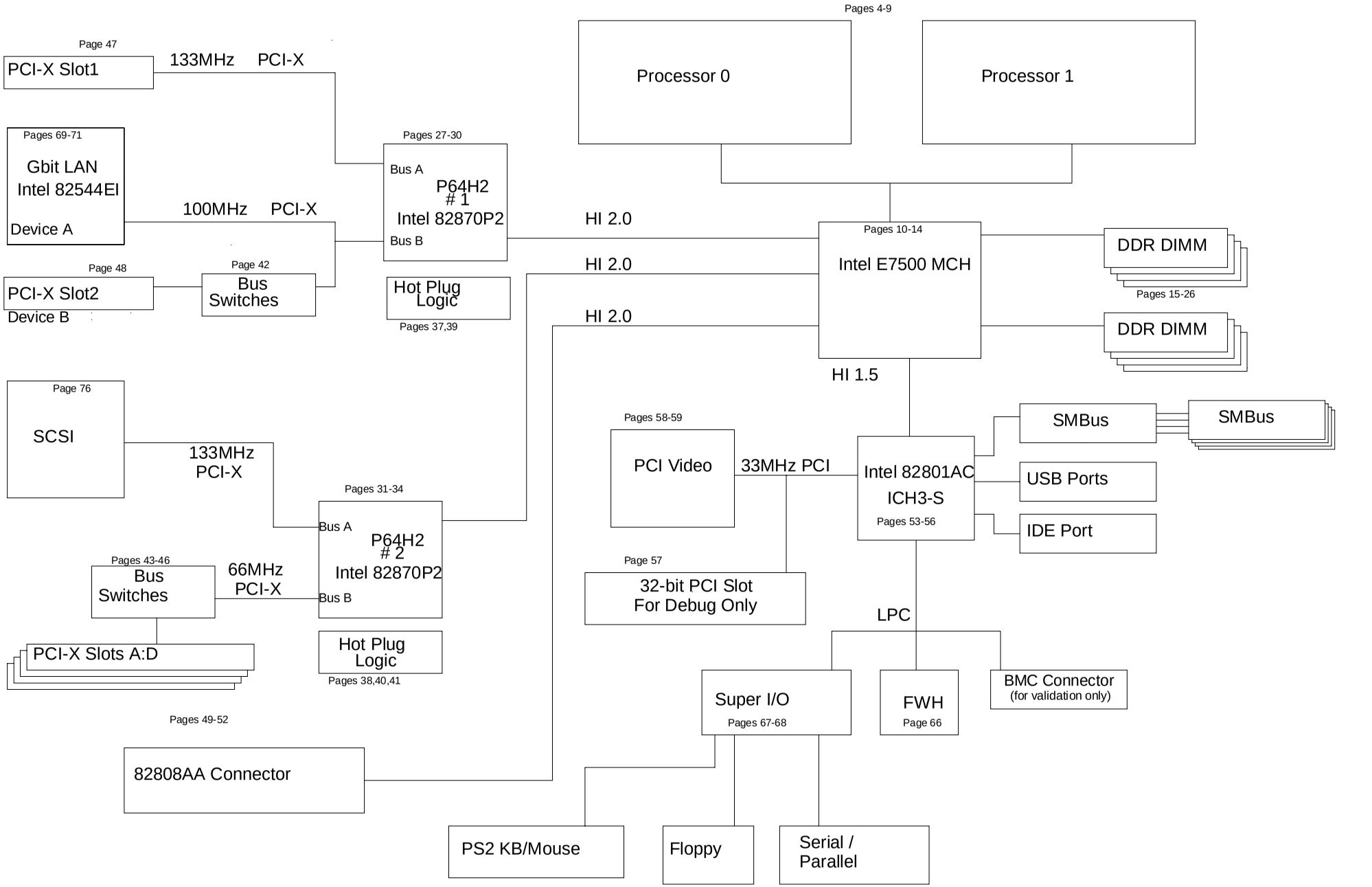

Simplified System Block Diagram

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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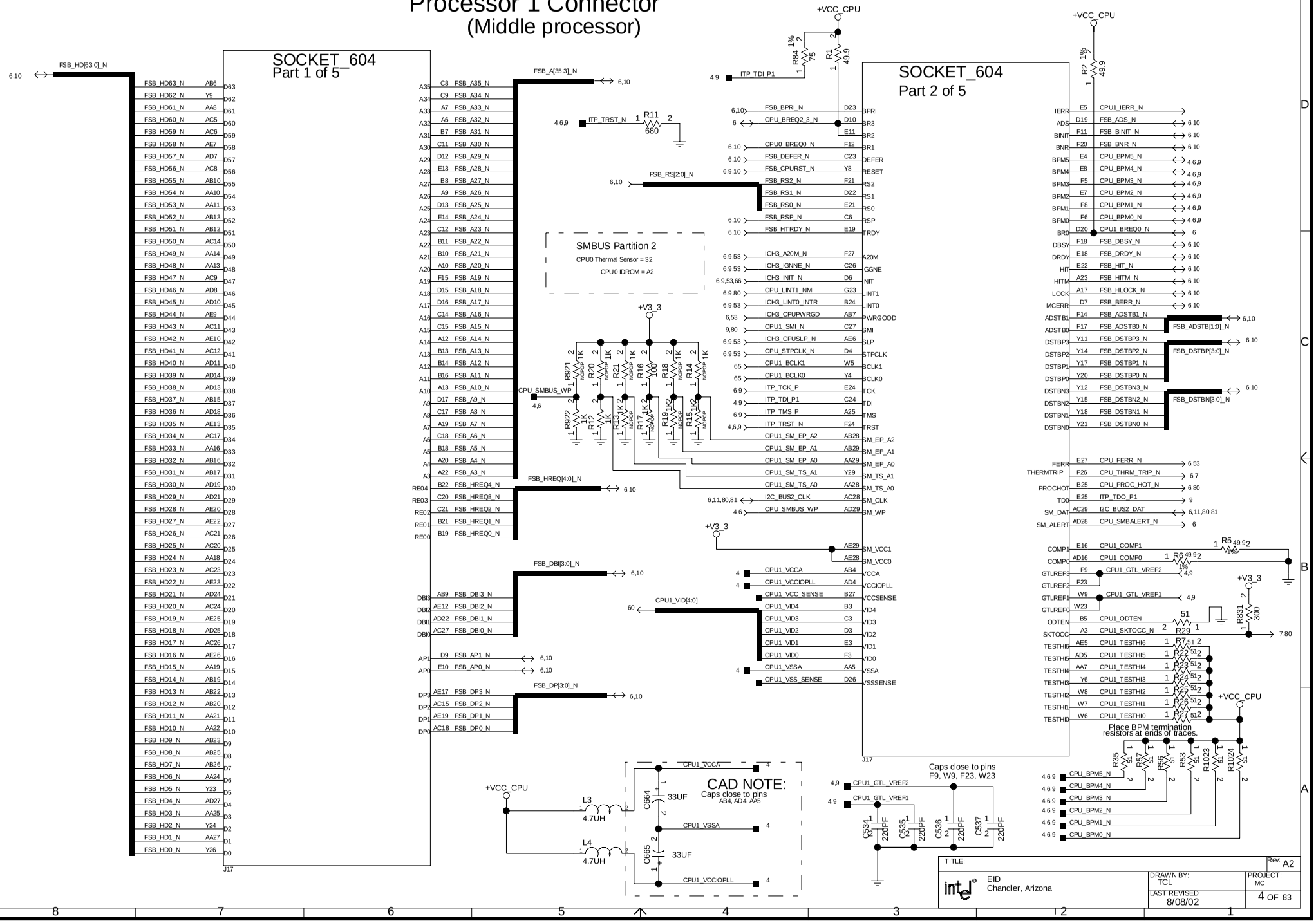
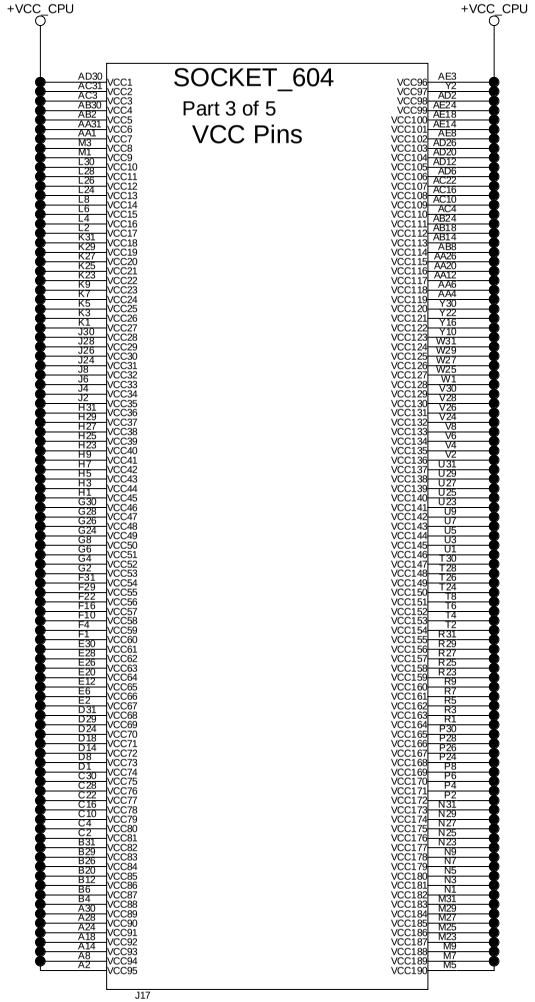
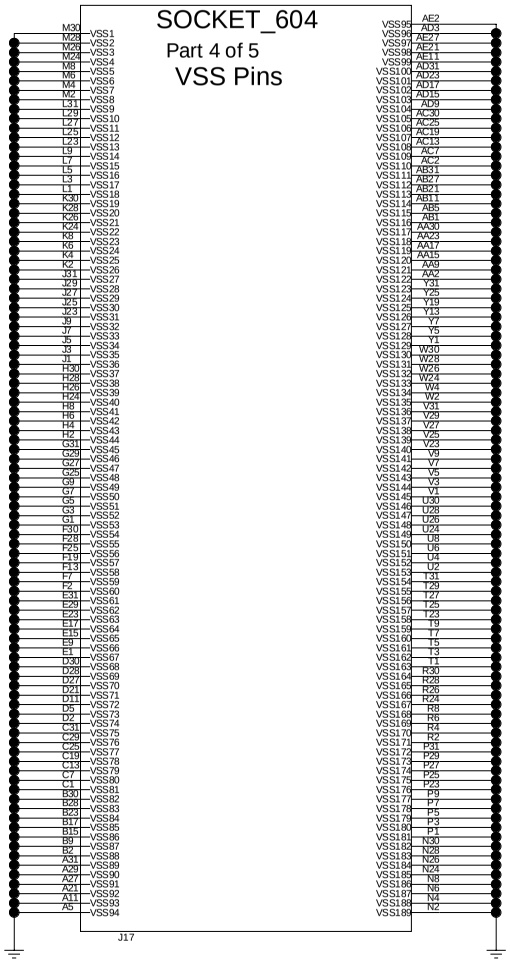
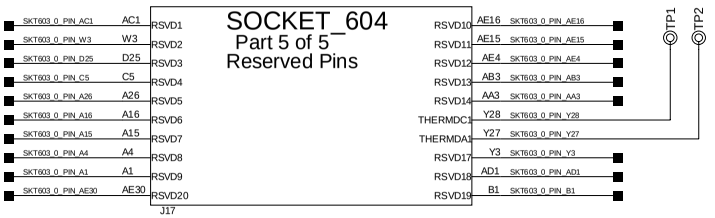
Processor 1 Connector
(Middle processor)



Processor 1 Connector







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intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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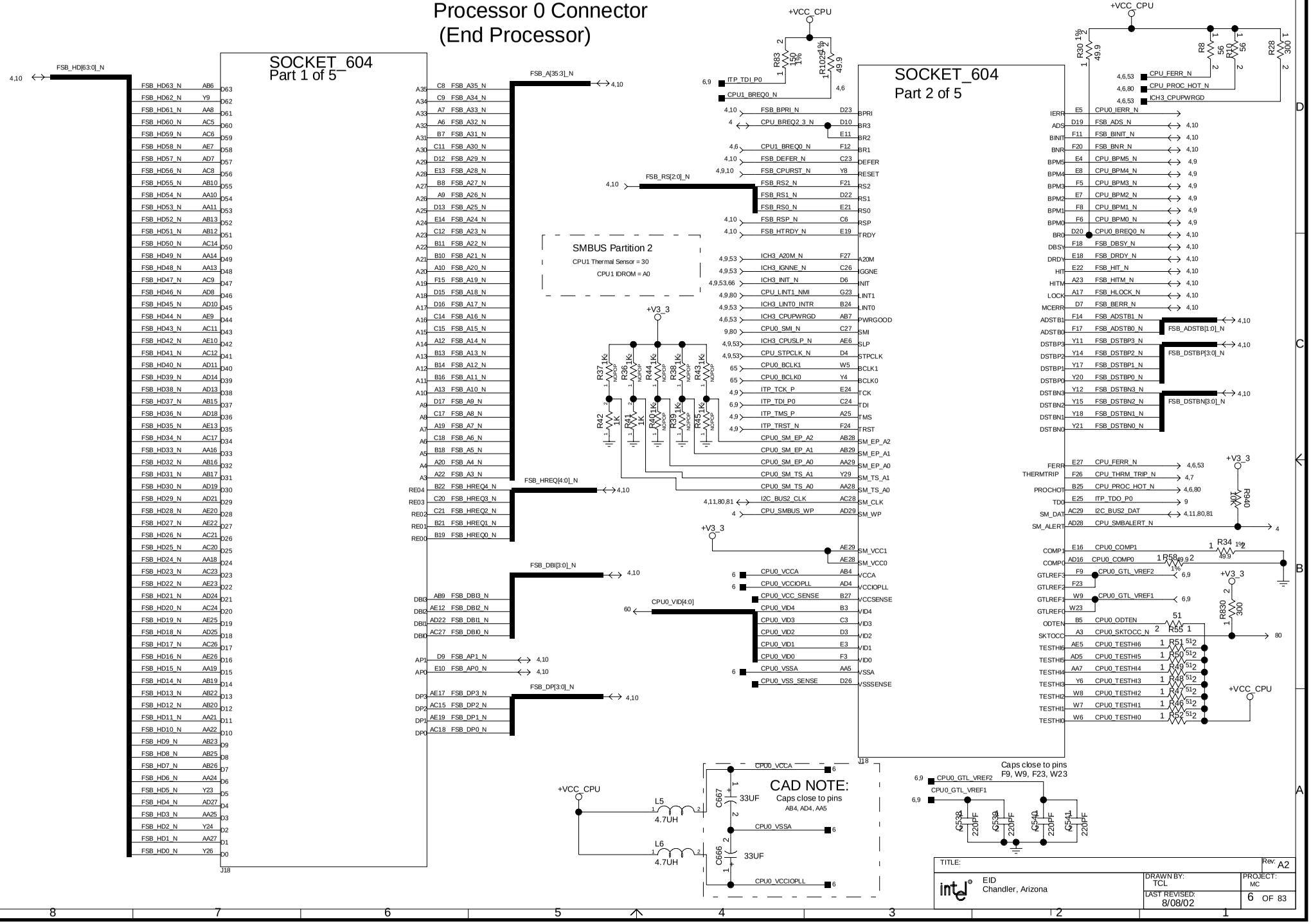
Processor 0 Connector (End Processor)



TITLE:

Rev: A2

intel EID Chandler, Arizona

DRAWN BY: TCL

PROJECT: MC

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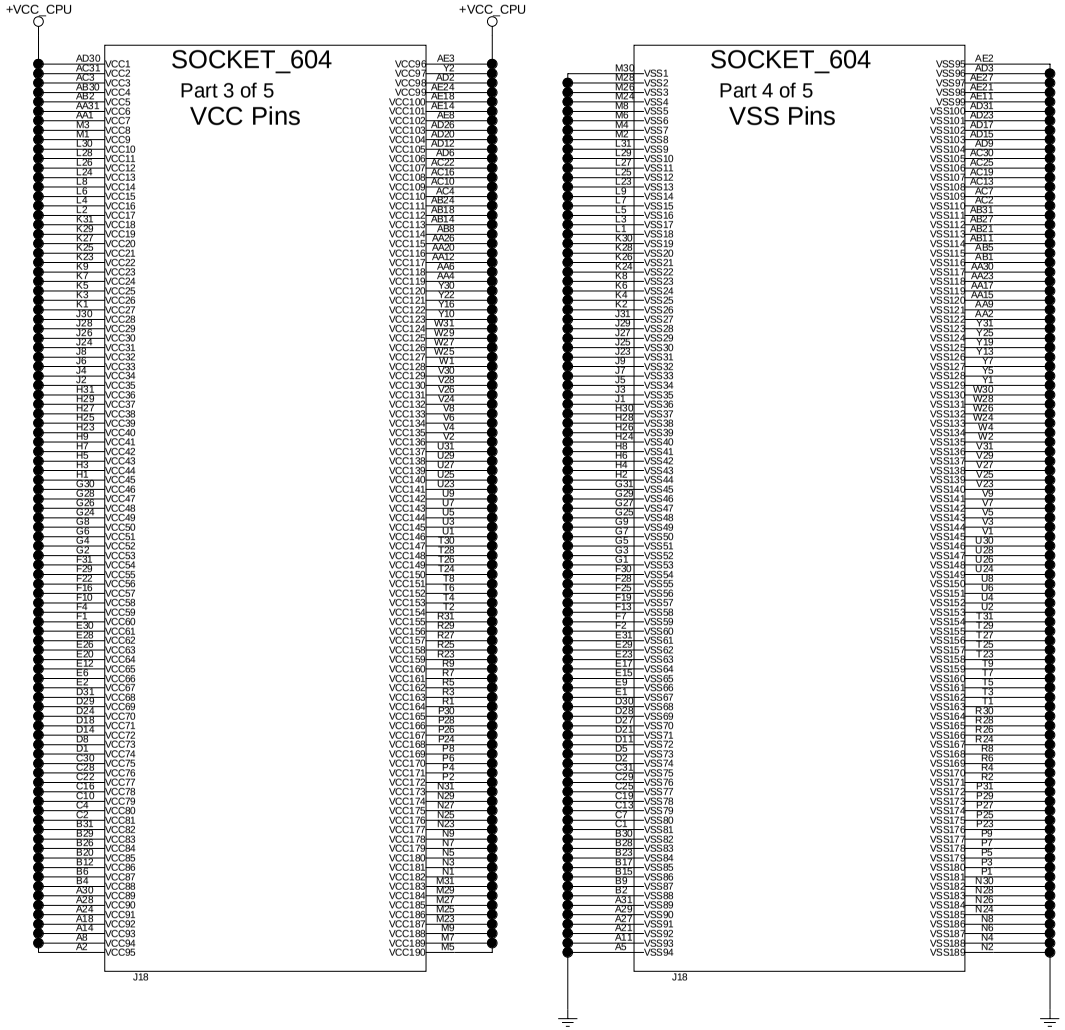
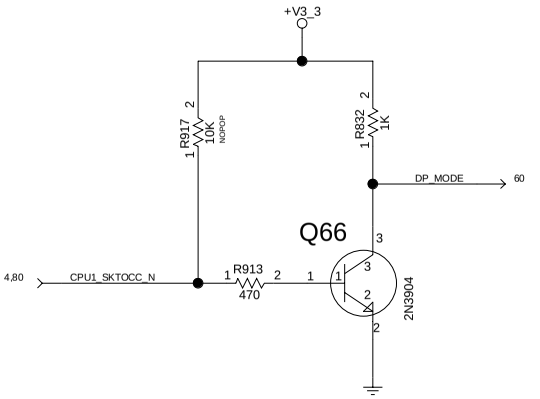
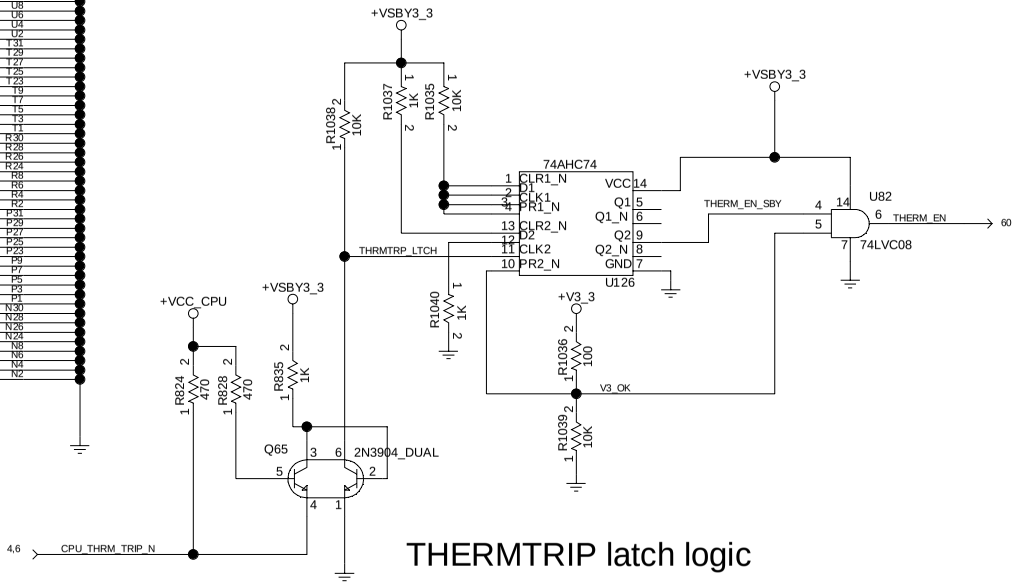
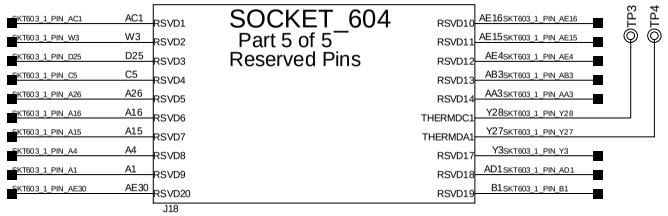
Processor 0 Connector







THERMTRIP latch logic



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intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
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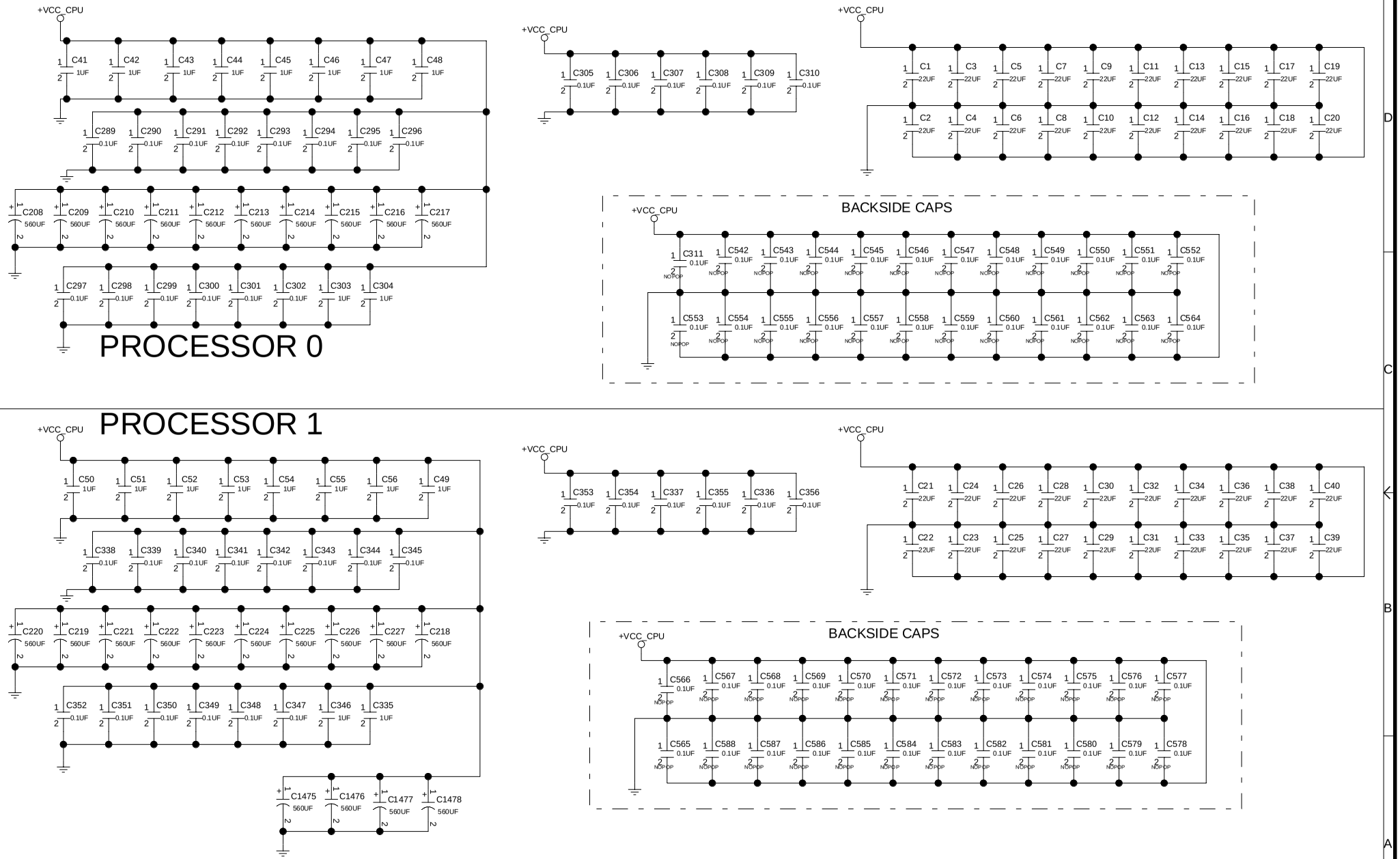

PROCESSOR 0/1 DECOUPLING

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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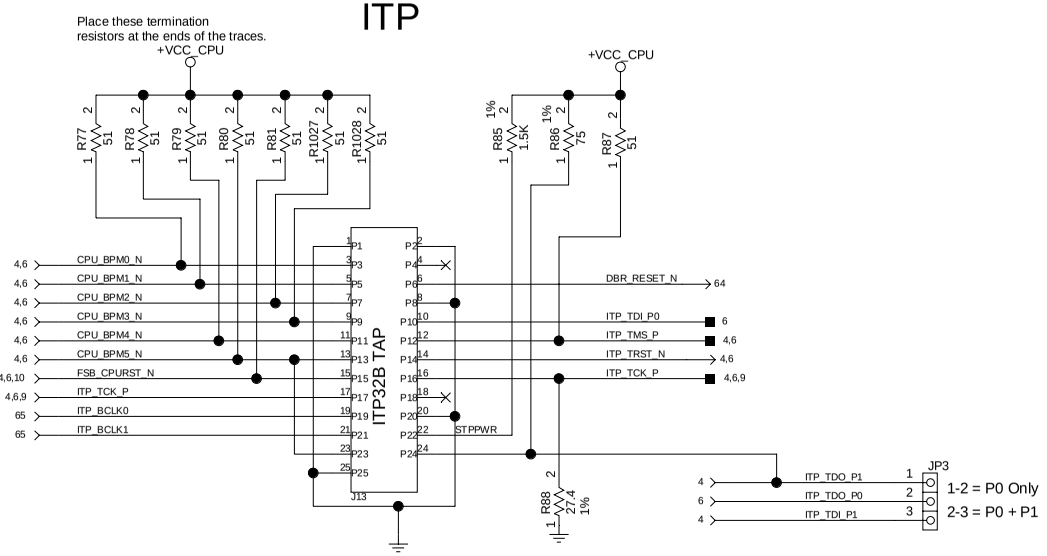
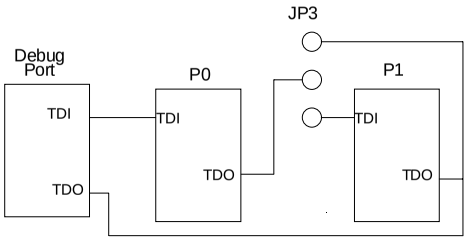
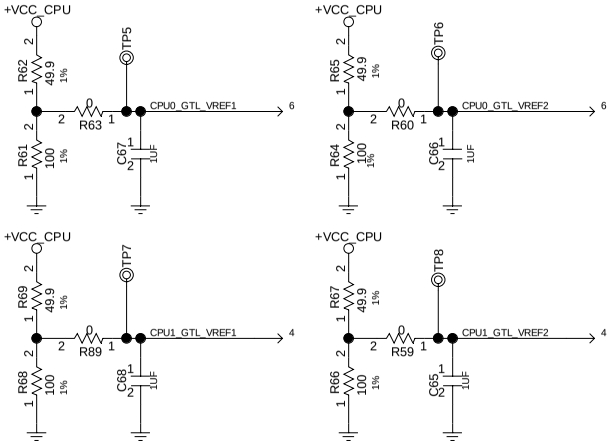
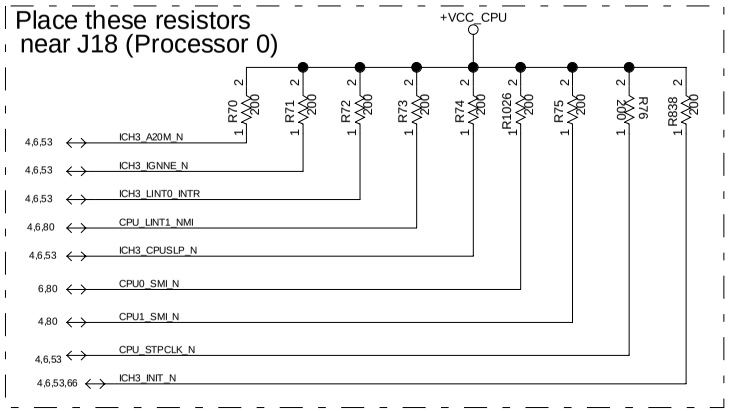
ITP





VREF circuits for GTL+





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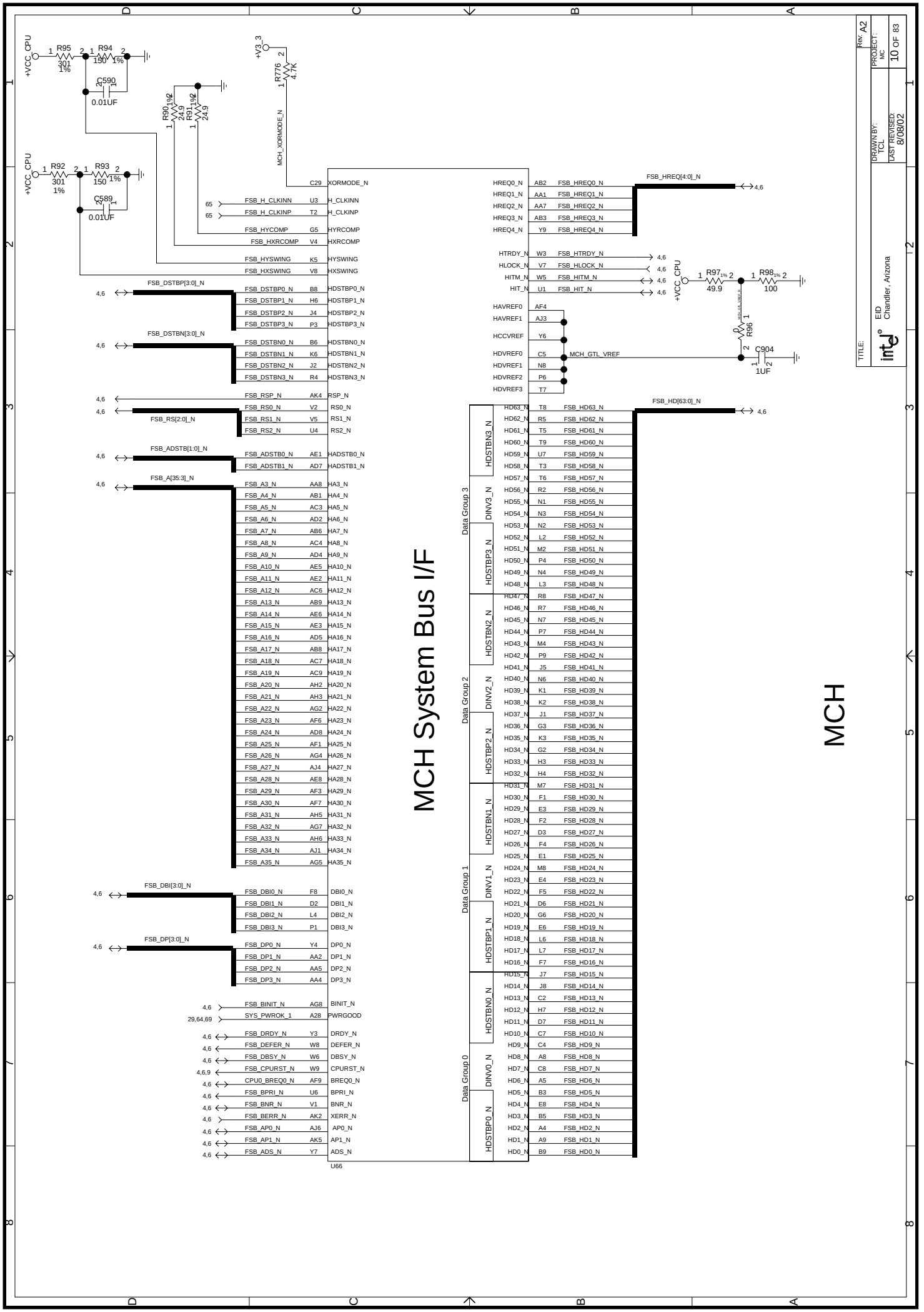
MCH System Bus I/F
MCH
U66
+VCC_CPU
R95 301 1%
R94 150 1%
C590 0.01UF
R92 301 1%
R93 150 1%
C589 0.01UF
+V3_3
R776 4.7K
R90 24.9 1%
R91 24.9 1%
MCH_XORMODE_N
C29 XORMODE_N
FSB_H_CLKINN U3 H_CLKINN
FSB_H_CLKINP T2 H_CLKINP
FSB_HYCOMP G5 HYRCOMP
FSB_HXRCOMP V4 HXRCOMP
FSB_HYSWING K5 HYSWING
FSB_HXSWING V8 HXSWING
FSB_DSTBP[3:0]_N
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FSB_DSTBP1_N H6 HDSTBP1_N
FSB_DSTBP2_N J4 HDSTBP2_N
FSB_DSTBP3_N P3 HDSTBP3_N
FSB_DSTBN[3:0]_N
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FSB_DSTBN1_N K6 HDSTBN1_N
FSB_DSTBN2_N J2 HDSTBN2_N
FSB_DSTBN3_N R4 HDSTBN3_N
FSB_RSP_N AK4 RSP_N
FSB_RS0_N V2 RS0_N
FSB_RS1_N V5 RS1_N
FSB_RS2_N U4 RS2_N
FSB_RS[2:0]_N
FSB_ADSTB[1:0]_N
FSB_ADSTB0_N AE1 HADSTB0_N
FSB_ADSTB1_N AD7 HADSTB1_N
FSB_A[35:3]_N
FSB_A3_N AA8 HA3_N
FSB_A4_N AB1 HA4_N
FSB_A5_N AC3 HA5_N
FSB_A6_N AD2 HA6_N
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FSB_A8_N AC4 HA8_N
FSB_A9_N AD4 HA9_N
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FSB_DBI[3:0]_N
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FSB_DBI2_N L4 DBI2_N
FSB_DBI3_N P1 DBI3_N
FSB_DP[3:0]_N
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FSB_DP2_N AA5 DP2_N
FSB_DP3_N AA4 DP3_N
FSB_BINIT_N AG8 BINIT_N
SYS_PWROK_1 A28 PWRGOOD
FSB_DRDY_N Y3 DRDY_N
FSB_DEFER_N W8 DEFER_N
FSB_DBSY_N W6 DBSY_N
FSB_CPURST_N W9 CPURST_N
CPU0_BREQ0_N AF9 BREQ0_N
FSB_BPRI_N U6 BPRI_N
FSB_BNR_N V1 BNR_N
FSB_BERR_N AK2 XERR_N
FSB_AP0_N AJ6 AP0_N
FSB_AP1_N AK5 AP1_N
FSB_ADS_N Y7 ADS_N
HREQ0_N AB2 FSB_HREQ0_N
HREQ1_N AA1 FSB_HREQ1_N
HREQ2_N AA7 FSB_HREQ2_N
HREQ3_N AB3 FSB_HREQ3_N
HREQ4_N Y9 FSB_HREQ4_N
FSB_HREQ[4:0]_N
HTRDY_N W3 FSB_HTRDY_N
HLOCK_N V7 FSB_HLOCK_N
HITM_N W5 FSB_HITM_N
HIT_N U1 FSB_HIT_N
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HAVREF1 AJ3
HCCVREF Y6
HDVREF0 C5
HDVREF1 N8
HDVREF2 P6
HDVREF3 T7
MCH_GTL_VREF
R97 49.9
R98 100
R96 0
C904 1UF
FSB_HD[63:0]_N
Data Group 3
Data Group 2
Data Group 1
Data Group 0
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DINV3_N
HDSTBP3_N
HDSTBN2_N
DINV2_N
HDSTBP2_N
HDSTBN1_N
DINV1_N
HDSTBP1_N
HDSTBN0_N
DINV0_N
HDSTBP0_N
HD63_N T8 FSB_HD63_N
HD62_N R5 FSB_HD62_N
HD61_N T5 FSB_HD61_N
HD60_N T9 FSB_HD60_N
HD59_N U7 FSB_HD59_N
HD58_N T3 FSB_HD58_N
HD57_N T6 FSB_HD57_N
HD56_N R2 FSB_HD56_N
HD55_N N1 FSB_HD55_N
HD54_N N3 FSB_HD54_N
HD53_N N2 FSB_HD53_N
HD52_N L2 FSB_HD52_N
HD51_N M2 FSB_HD51_N
HD50_N P4 FSB_HD50_N
HD49_N N4 FSB_HD49_N
HD48_N L3 FSB_HD48_N
HD47_N R8 FSB_HD47_N
HD46_N R7 FSB_HD46_N
HD45_N N7 FSB_HD45_N
HD44_N P7 FSB_HD44_N
HD43_N M4 FSB_HD43_N
HD42_N P9 FSB_HD42_N
HD41_N J5 FSB_HD41_N
HD40_N N6 FSB_HD40_N
HD39_N K1 FSB_HD39_N
HD38_N K2 FSB_HD38_N
HD37_N J1 FSB_HD37_N
HD36_N G3 FSB_HD36_N
HD35_N K3 FSB_HD35_N
HD34_N G2 FSB_HD34_N
HD33_N H3 FSB_HD33_N
HD32_N H4 FSB_HD32_N
HD31_N M7 FSB_HD31_N
HD30_N F1 FSB_HD30_N
HD29_N E3 FSB_HD29_N
HD28_N F2 FSB_HD28_N
HD27_N D3 FSB_HD27_N
HD26_N F4 FSB_HD26_N
HD25_N E1 FSB_HD25_N
HD24_N M8 FSB_HD24_N
HD23_N E4 FSB_HD23_N
HD22_N F5 FSB_HD22_N
HD21_N D6 FSB_HD21_N
HD20_N G6 FSB_HD20_N
HD19_N E6 FSB_HD19_N
HD18_N L6 FSB_HD18_N
HD17_N L7 FSB_HD17_N
HD16_N F7 FSB_HD16_N
HD15_N J7 FSB_HD15_N
HD14_N J8 FSB_HD14_N
HD13_N C2 FSB_HD13_N
HD12_N H7 FSB_HD12_N
HD11_N D7 FSB_HD11_N
HD10_N C7 FSB_HD10_N
HD9_N C4 FSB_HD9_N
HD8_N A8 FSB_HD8_N
HD7_N C8 FSB_HD7_N
HD6_N A5 FSB_HD6_N
HD5_N B3 FSB_HD5_N
HD4_N E8 FSB_HD4_N
HD3_N B5 FSB_HD3_N
HD2_N A4 FSB_HD2_N
HD1_N A9 FSB_HD1_N
HD0_N B9 FSB_HD0_N
Rev: A2
PROJECT: MC
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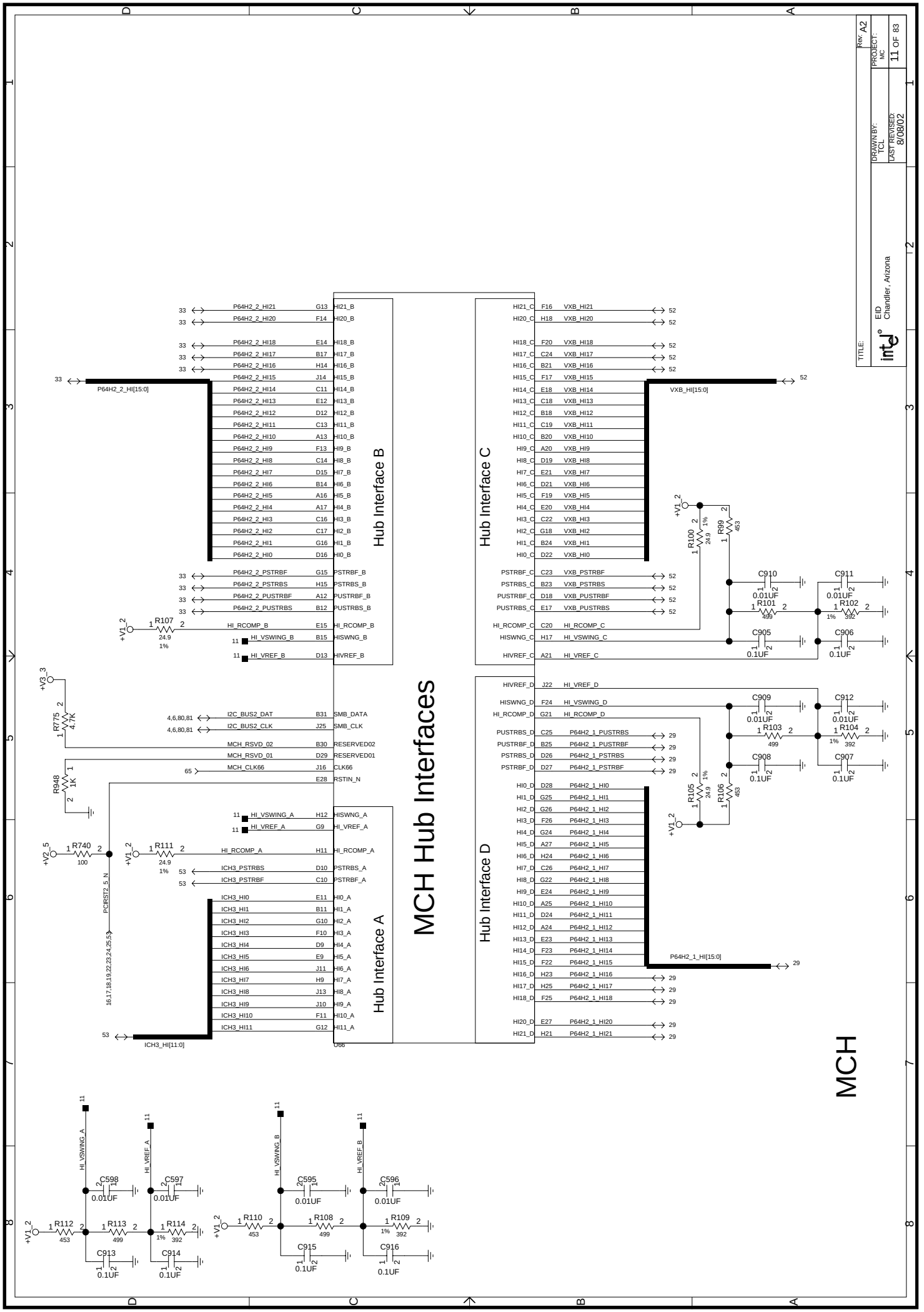
DRAWN BY: TCL
LAST REVISED: 8/08/02
TITLE:
EID
Chandler, Arizona


MCH Hub Interfaces
Hub Interface A
Hub Interface B
Hub Interface C
Hub Interface D
MCH
P64H2_2_HI[15:0]
ICH3_HI[11:0]
VXB_HI[15:0]
P64H2_1_HI[15:0]
HI_VSWING_A
HI_VREF_A
HI_VSWING_B
HI_VREF_B
TITLE:
Intel
EID
Chandler, Arizona
DRAWN BY:
TCL
LAST REVISED:
8/08/02
PROJECT:
MC
11 OF 83
Rev: A2

MCH DDR A
MCH DDR Channel A
DDRA_DQ0 AF22 DQ0_A
DDRA_DQ1 AN28 DQ1_A
DDRA_DQ2 AE21 DQ2_A
DDRA_DQ3 AH22 DQ3_A
DDRA_DQS0 AM27 DQS0_A
DDRA_DQS9 AF21 DQS9_A
DDRA_DQ4 AN29 DQ4_A
DDRA_DQ5 AM28 DQ5_A
DDRA_DQ6 AL26 DQ6_A
DDRA_DQ7 AL25 DQ7_A
DDRA_DQ8 AN25 DQ8_A
DDRA_DQ9 AM24 DQ9_A
DDRA_DQ10 AG21 DQ10_A
DDRA_DQ11 AE20 DQ11_A
DDRA_DQS1 AL23 DQS1_A
DDRA_DQS10 AK23 DQS10_A
DDRA_DQ12 AM25 DQ12_A
DDRA_DQ13 AK24 DQ13_A
DDRA_DQ14 AL22 DQ14_A
DDRA_DQ15 AJ22 DQ15_A
DDRA_DQ16 AK19 DQ16_A
DDRA_DQ17 AL19 DQ17_A
DDRA_DQ18 AN17 DQ18_A
DDRA_DQ19 AF18 DQ19_A
DDRA_DQS2 AG18 DQS2_A
DDRA_DQS11 AK18 DQS11A
DDRA_DQ20 AN20 DQ20_A
DDRA_DQ21 AM19 DQ21_A
DDRA_DQ22 AL17 DQ22_A
DDRA_DQ23 AJ18 DQ23_A
DDRA_DQ24 AF19 DQ24_A
DDRA_DQ25 AH19 DQ25_A
DDRA_DQ26 AM21 DQ26_A
DDRA_DQ27 AL20 DQ27_A
DDRA_DQS3 AE18 DQS3_A
DDRA_DQS12 AK20 DQS12_A
DDRA_DQ28 AH20 DQ28_A
DDRA_DQ29 AJ21 DQ29_A
DDRA_DQ30 AN21 DQ30_A
DDRA_DQ31 AJ19 DQ31_A
DDRA_DQ32 AL14 DQ32_A
DDRA_DQ33 AM13 DQ33A
DDRA_DQ34 AJ15 DQ34_A
DDRA_DQ35 AF15 DQ35_A
DDRA_DQS4 AL13 DQS4_A
DDRA_DQS13 AJ13 DQS13_A
DDRA_DQ36 AK14 DQ36_A
DDRA_DQ37 AN13 DQ37_A
DDRA_DQ38 AH14 DQ38_A
DDRA_DQ39 AG14 DQ39_A
DDRA_DQ40 AE14 DQ40_A
DDRA_DQ41 AH13 DQ41_A
DDRA_DQ42 AN12 DQ42_A
DDRA_DQ43 AL11 DQ43_A
DDRA_DQS5 AM12 DQS5_A
DDRA_DQS14 AK12 DQS14_A
DDRA_DQ44 AE15 DQ44_A
DDRA_DQ45 AF13 DQ45_A
DDRA_DQ46 AJ12 DQ46_A
DDRA_DQ47 AM10 DQ47_A
DDRA_DQ48 AE12 DQ48_A
DDRA_DQ49 AH11 DQ49_A
DDRA_DQ50 AG11 DQ50_A
DDRA_DQ51 AN5 DQ51_A
DDRA_DQS6 AL8 DQS6_A
DDRA_DQS15 AM7 DQS15_A
DDRA_DQ52 AG12 DQ52_A
DDRA_DQ53 AF12 DQ53_A
DDRA_DQ54 AM9 DQ54_A
DDRA_DQ55 AM6 DQ55_A
DDRA_DQ56 AG10 DQ56_A
DDRA_DQ57 AJ9 DQ57_A
DDRA_DQ58 AM3 DQ58_A
DDRA_DQ59 AM2 DQ59_A
DDRA_DQS7 AL6 DQS7_A
DDRA_DQS16 AH9 DQS16_A
DDRA_DQ60 AH10 DQ60_A
DDRA_DQ61 AE11 DQ61_A
DDRA_DQ62 AL5 DQ62_A
DDRA_DQ63 AM4 DQ63_A
DDRA_CB0 AE16 CB0_A
DDRA_CB1 AH16 CB1_A
DDRA_CB2 AL16 CB2_A
DDRA_CB3 AK15 CB3_A
DDRA_DQS8 AJ16 DQS8_A
DDRA_DQS17 AF16 DQS17_A
DDRA_CB4 AE17 CB4_A
DDRA_CB5 AG17 CB5_A
DDRA_CB6 AM15 CB6_A
DDRA_CB7 AG15 CB7_A
Low Nibble Data Group 0
High Nibble Data Group 0
Low Nibble Data Group 1
High Nibble Data Group 1
Low Nibble Data Group 2
High Nibble Data Group 2
Low Nibble Data Group 3
High Nibble Data Group 3
Low Nibble Data Group 4
High Nibble Data Group 4
Low Nibble Data Group 5
High Nibble Data Group 5
Low Nibble Data Group 6
High Nibble Data Group 6
Low Nibble Data Group 7
High Nibble Data Group 7
Low Nibble Check Bits
High Nibble Check Bits
U66
Address Bus
WE_N_A AE23 DDRA_WE_N_R 16,17,18,19,20
CAS_N_A AE22 DDRA_CAS_N_R 16,17,18,19,20
RAS_N_A AN24 DDRA_RAS_N_R 16,17,18,19,20
MA0_A AF24 DDRA_MA0_R 16,17,18,19,20
MA1_A AK26 DDRA_MA1_R 16,17,18,19,20
MA2_A AH26 DDRA_MA2_R 16,17,18,19,20
MA3_A AJ27 DDRA_MA3_R 16,17,18,19,20
MA4_A AG27 DDRA_MA4_R 16,17,18,19,20
MA5_A AH28 DDRA_MA5_R 16,17,18,19,20
MA6_A AL28 DDRA_MA6_R 16,17,18,19,20
MA7_A AL29 DDRA_MA7_R 16,17,18,19,20
MA8_A AK29 DDRA_MA8_R 16,17,18,19,20
MA9_A AM30 DDRA_MA9_R 16,17,18,19,20
MA10_A AJ24 DDRA_MA10_R 16,17,18,19,20
MA11_A AK30 DDRA_MA11_R 16,17,18,19,20
MA12_A AM31 DDRA_MA12_R 16,17,18,19,20
BA1_A AH23 DDRA_BA1_R 16,17,18,19,26
BA0_A AL31 DDRA_BA0_R 16,17,18,19,20
Chip Select
CS7_N_A AL2 DDRA_CS7_N_R 19,20
CS6_N_A AL3 DDRA_CS6_N_R 19,20
CS5_N_A AK7 DDRA_CS5_N_R 18,26
CS4_N_A AN8 DDRA_CS4_N_R 18,26
CS3_N_A AH8 DDRA_CS3_N_R 17,20
CS2_N_A AL10 DDRA_CS2_N_R 17,20
CS1_N_A AK11 DDRA_CS1_N_R 16,20
CS0_N_A AE13 DDRA_CS0_N_R 16,20
VTT_DDR
R841 47
RCVEN_IN_A AM22 DDRA_RCV_EN_IN 20
RCVEN_OUT_A AG20 DDRA_RCV_EN_OUT 20
DDRCOMP_A AH17 DDRA_DRCOMP
DDRCVOH_A AK17 DDRCVOH_A
DDRCVOL_A AN16 DDRCVOL_A
R115 6.81
C1669 0.1UF
C1668 0.1UF
C1667 0.1UF
C1666 0.1UF
R524 6.98K 1%
C779 0.01UF
C780 0.1UF
+V2_5
C778 0.01UF
C777 0.1UF
R523 6.98K 1%
R522 13K
R521 13K
CKE_A AE19 R117 0 DDRA_CKE0 16,17,18,19,20
RESERVED AM18 R118 0 DDRA_CKE1 16,17,18,19,20
Command Clock
CMDCLK3_A AE25 DDRA_CMDCLK3 19
CMDCLK3_N_A AE24 DDRA_CMDCLK3_N 19
CMDCLK2_A AG26 DDRA_CMDCLK2 18
CMDCLK2_N_A AF25 DDRA_CMDCLK2_N 18
CMDCLK1_A AJ25 DDRA_CMDCLK1 17
CMDCLK1_N_A AH25 DDRA_CMDCLK1_N 17
CMDCLK0_A AG24 DDRA_CMDCLK0 16
CMDCLK0_N_A AG23 DDRA_CMDCLK0_N 16
Voltage Ref
DDRVREF5_A AJ28
DDRVREF4_A AK27
DDRVREF3_A AK21
DDRVREF2_A AM16
DDRVREF1_A AL9
DDRVREF0_A AJ7
R923 0
R924 0
R925 0
DDRA_VREF_FLT_1
DDRA_VREF_FLT_2
DDRA_VREF_FLT_3
C1143 0.1UF
C1144 0.1UF
C1145 0.1UF
VREF_DDR_MCH
13,62
TITLE:
intel
EID
Chandler, Arizona
DRAWN BY: TCL
LAST REVISED: 8/08/02
PROJECT: MC
Rev: A2
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MCH DDR B
MCH DDR Channel B
DDRB_DQ0 F33 DQ0_B
DDRB_DQ1 K30 DQ1_B
DDRB_DQ2 J32 DQ2_B
DDRB_DQ3 N25 DQ3_B
DDRB_DQS0 L30 DQS0_B
DDRB_DQS9 H31 DQS9_B
DDRB_DQ4 N27 DQ4_B
DDRB_DQ5 G32 DQ5_B
DDRB_DQ6 M29 DQ6_B
DDRB_DQ7 N26 DQ7_B
DDRB_DQ8 J33 DQ8_B
DDRB_DQ9 K32 DQ9_B
DDRB_DQ10 P27 DQ10_B
DDRB_DQ11 P25 DQ11_B
DDRB_DQS1 M31 DQS1_B
DDRB_DQS10 N29 DQS10_B
DDRB_DQ12 J31 DQ12_B
DDRB_DQ13 L31 DQ13_B
DDRB_DQ14 P26 DQ14_B
DDRB_DQ15 P28 DQ15_B
DDRB_DQ16 T29 DQ16_B
DDRB_DQ17 T30 DQ17_B
DDRB_DQ18 U30 DQ18_B
DDRB_DQ19 T26 DQ19_B
DDRB_DQS2 U33 DQS2_B
DDRB_DQS11 U31 DQS11_B
DDRB_DQ20 R32 DQ20_B
DDRB_DQ21 T27 DQ21_B
DDRB_DQ22 V33 DQ22_B
DDRB_DQ23 V31 DQ23_B
DDRB_DQ24 P30 DQ24_B
DDRB_DQ25 P33 DQ25_B
DDRB_DQ26 R26 DQ26_B
DDRB_DQ27 T32 DQ27_B
DDRB_DQS3 R29 DQS3_B
DDRB_DQS12 R31 DQS12_B
DDRB_DQ28 N32 DQ28_B
DDRB_DQ29 P31 DQ29_B
DDRB_DQ30 R28 DQ30_B
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DDRB_DQS4 AE32 DQS4_B
DDRB_DQS13 AC30 DQS13_B
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DDRB_DQ40 AA29 DQ40_B
DDRB_DQ41 AB33 DQ41_B
DDRB_DQ42 V26 DQ42_B
DDRB_DQ43 AD31 DQ43_B
DDRB_DQS5 AC31 DQS5_B
DDRB_DQS14 AB30 DQS14_B
DDRB_DQ44 Y28 DQ44_B
DDRB_DQ45 AB32 DQ45_B
DDRB_DQ46 AB29 DQ46_B
DDRB_DQ47 V25 DQ47_B
DDRB_DQ48 Y25 DQ48_B
DDRB_DQ49 AB27 DQ49_B
DDRB_DQ50 AH32 DQ50_B
DDRB_DQ51 AH31 DQ51_B
DDRB_DQS6 AE28 DQS6_B
DDRB_DQS15 AD27 DQS15_B
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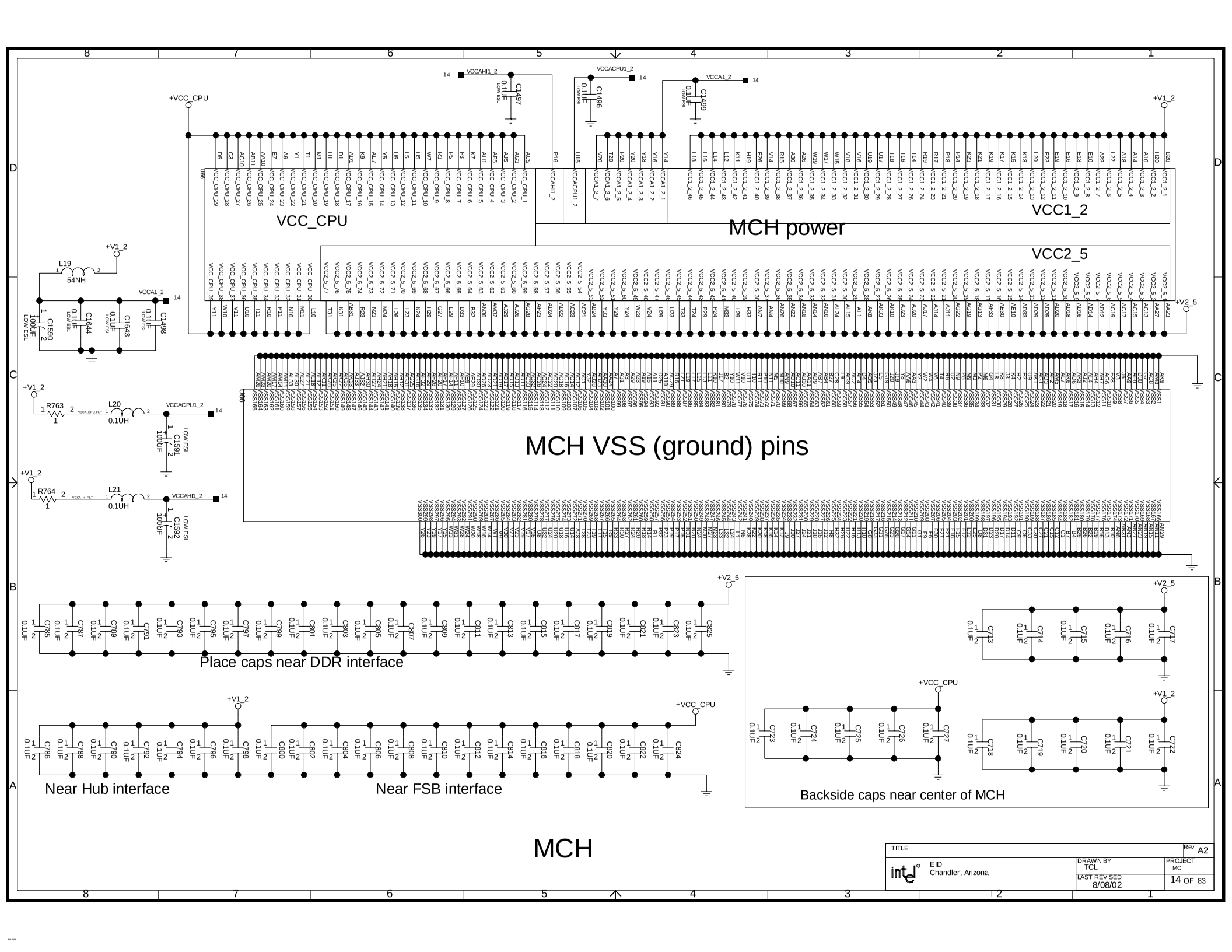
DDRB_DQ55 AH33 DQ55_B
DDRB_DQ56 AJ30 DQ56_B
DDRB_DQ57 AG29 DQ57_B
DDRB_DQ58 AB25 DQ58_B
DDRB_DQ59 AA25 DQ59_B
DDRB_DQS7 AE27 DQS7_B
DDRB_DQS16 AF28 DQS16_B
DDRB_DQ60 AL32 DQ60_B
DDRB_DQ61 AJ31 DQ61_B
DDRB_DQ62 AC27 DQ62_B
DDRB_DQ63 AB26 DQ63_B
DDRB_CB0 V28 CB0_B
DDRB_CB1 U25 CB1_B
DDRB_CB2 Y31 CB2_B
DDRB_CB3 AA33 CB3_B
DDRB_DQS8 W29 DQS8_B
DDRB_DQS17 Y30 DQS17_B
DDRB_CB4 U28 CB4_B
DDRB_CB5 U27 CB5_B
DDRB_CB6 AA31 CB6_B
DDRB_CB7 AA32 CB7_B
Low Nibble Data Group 0
High Nibble Data Group 0
Low Nibble Data Group 1
High Nibble Data Group 1
Low Nibble Data Group 2
High Nibble Data Group 2
Low Nibble Data Group 3
High Nibble Data Group 3
Low Nibble Data Group 4
High Nibble Data Group 4
Low Nibble Data Group 5
High Nibble Data Group 5
Low Nibble Data Group 6
High Nibble Data Group 6
Low Nibble Data Group 7
High Nibble Data Group 7
Low Nibble Check Bits
High Nibble Check Bits
U66
Address Bus
WE_N_B D32 DDRB_WE_N_R 22,23,24,25,26
CAS_N_B H28 DDRB_CAS_N_R 22,23,24,25,26
RAS_N_B V32 DDRB_RAS_N_R 20,22,23,24,25
MA0_B M26 DDRB_MA0_R 22,23,24,25,26
MA1_B K29 DDRB_MA1_R 22,23,24,25,26
MA2_B H30 DDRB_MA2_R 22,23,24,25,26
MA3_B G30 DDRB_MA3_R 22,23,24,25,26
MA4_B F32 DDRB_MA4_R 22,23,24,25,26
MA5_B G29 DDRB_MA5_R 22,23,24,25,26
MA6_B F31 DDRB_MA6_R 22,23,24,25,26
MA7_B E33 DDRB_MA7_R 22,23,24,25,26
MA8_B E31 DDRB_MA8_R 22,23,24,25,26
MA9_B F29 DDRB_MA9_R 22,23,24,25,26
MA10_B L25 DDRB_MA10_R 20,22,23,24,25
MA11_B C31 DDRB_MA11_R 22,23,24,25,26
MA12_B C32 DDRB_MA12_R 22,23,24,25,26
BA1_B H27 DDRB_BA1_R 22,23,24,25,26
BA0_B K26 DDRB_BA0_R 22,23,24,25,26
Chip Select
CS7_N_B Y27 DDRB_CS7_N_R 20,25
CS6_N_B AD28 DDRB_CS6_N_R 20,25
CS5_N_B AE26 DDRB_CS5_N_R 24,26
CS4_N_B AE31 DDRB_CS4_N_R 24,26
CS3_N_B AF27 DDRB_CS3_N_R 23,26
CS2_N_B AF30 DDRB_CS2_N_R 23,26
CS1_N_B AK32 DDRB_CS1_N_R 22,26
CS0_N_B AH29 DDRB_CS0_N_R 22,26
VTT_DDR
R843 47
RCVEN_IN_B N30 DDRB_RCV_EN_IN 26
RCVEN_OUT_B R25 DDRB_RCV_EN_OUT 26
DDRCOMP_B W30 DDRB_DRCOMP
R120 6.81
DDRCVOH_B W32 DDRCVOH_B
DDRCVOL_B V29 DDRCVOL_B
R527 6.98K 1%
C782 0.01UF
C781 0.1UF
C784 0.01UF
C783 0.1UF
+V2_5
R526 6.98K 1%
R525 13K
R528 13K
RESERVED K33 R123 0 DDRB_CKE1 22,23,24,25,26
CKE_B M32 R124 0 DDRB_CKE0 22,23,24,25,26
Command Clock
CMDCLK3_B K27 DDRB_CMDCLK3 25
CMDCLK3_N_B L27 DDRB_CMDCLK3_N 25
CMDCLK2_B J26 DDRB_CMDCLK2 24
CMDCLK2_N_B K25 DDRB_CMDCLK2_N 24
CMDCLK1_B L28 DDRB_CMDCLK1 23
CMDCLK1_N_B M28 DDRB_CMDCLK1_N 23
CMDCLK0_B J29 DDRB_CMDCLK0 22
CMDCLK0_N_B J28 DDRB_CMDCLK0_N 22
Voltage Ref
DDRVREF5_B E30
DDRVREF4_B M25
DDRVREF3_B N33
DDRVREF2_B U26
DDRVREF1_B AG32
DDRVREF0_B AC25
R928 0
R927 0
R926 0
DDRB_VREF_FLT.1
DDRB_VREF_FLT.2
DDRB_VREF_FLT.3
C1146 0.1UF
C1147 0.1UF
C1148 0.1UF
VREF_DDR_MCH
12,62
TITLE:
intel
EID
Chandler, Arizona
DRAWN BY: TCL
LAST REVISED: 8/08/02
PROJECT: MC
13 OF 83
Rev: A2


VCC_CPU
VCC1_2
MCH power
VCC2_5
MCH VSS (ground) pins
Place caps near DDR interface
Near Hub interface
Near FSB interface
Backside caps near center of MCH
MCH
+VCC_CPU
+V1_2
+V2_5
VCCAHI1_2
VCCACPU1_2
VCCA1_2
TITLE:
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EID
Chandler, Arizona
DRAWN BY: TCL
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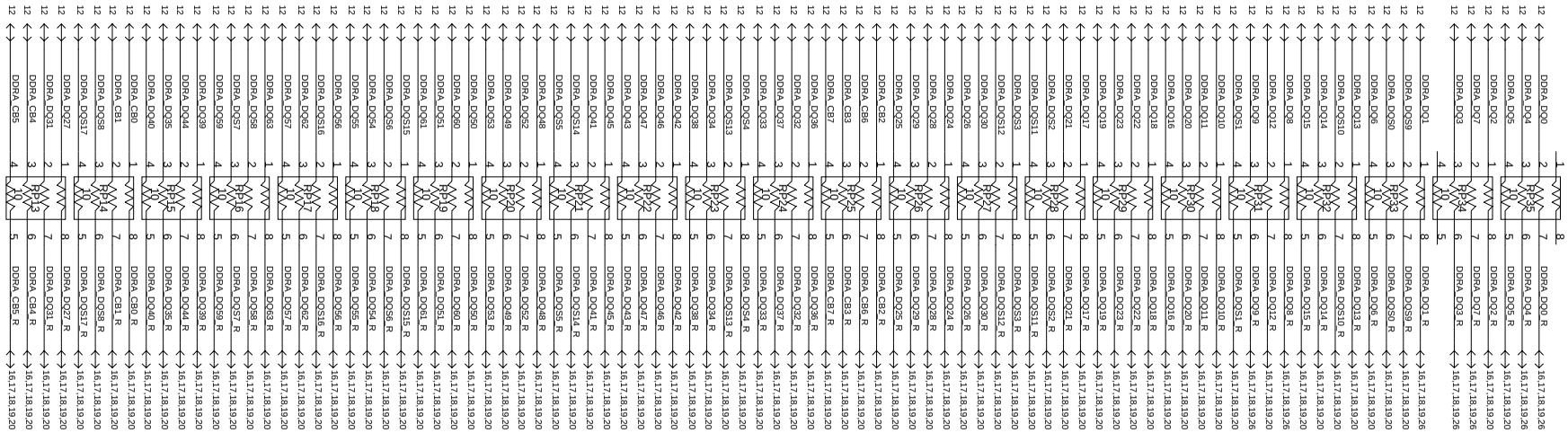
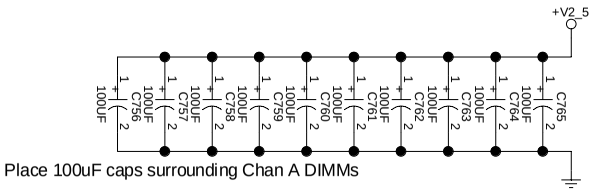
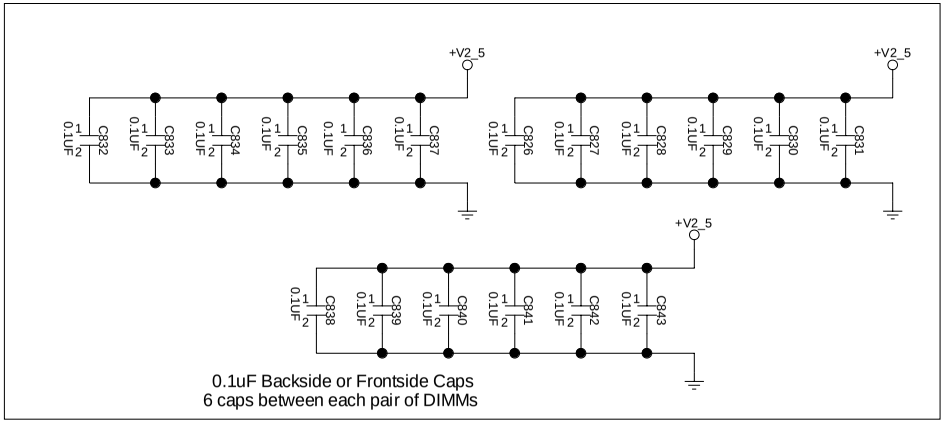
DDR Channel A Series Resistors

Place near DIMM A-1





Place 100uF caps surrounding Chan A DIMMs



0.1uF Backside or Frontside Caps
6 caps between each pair of DIMMs

CAD Note: All Caps should have direct attatchment to 2.5V plane, and 2 vias to GND.

TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
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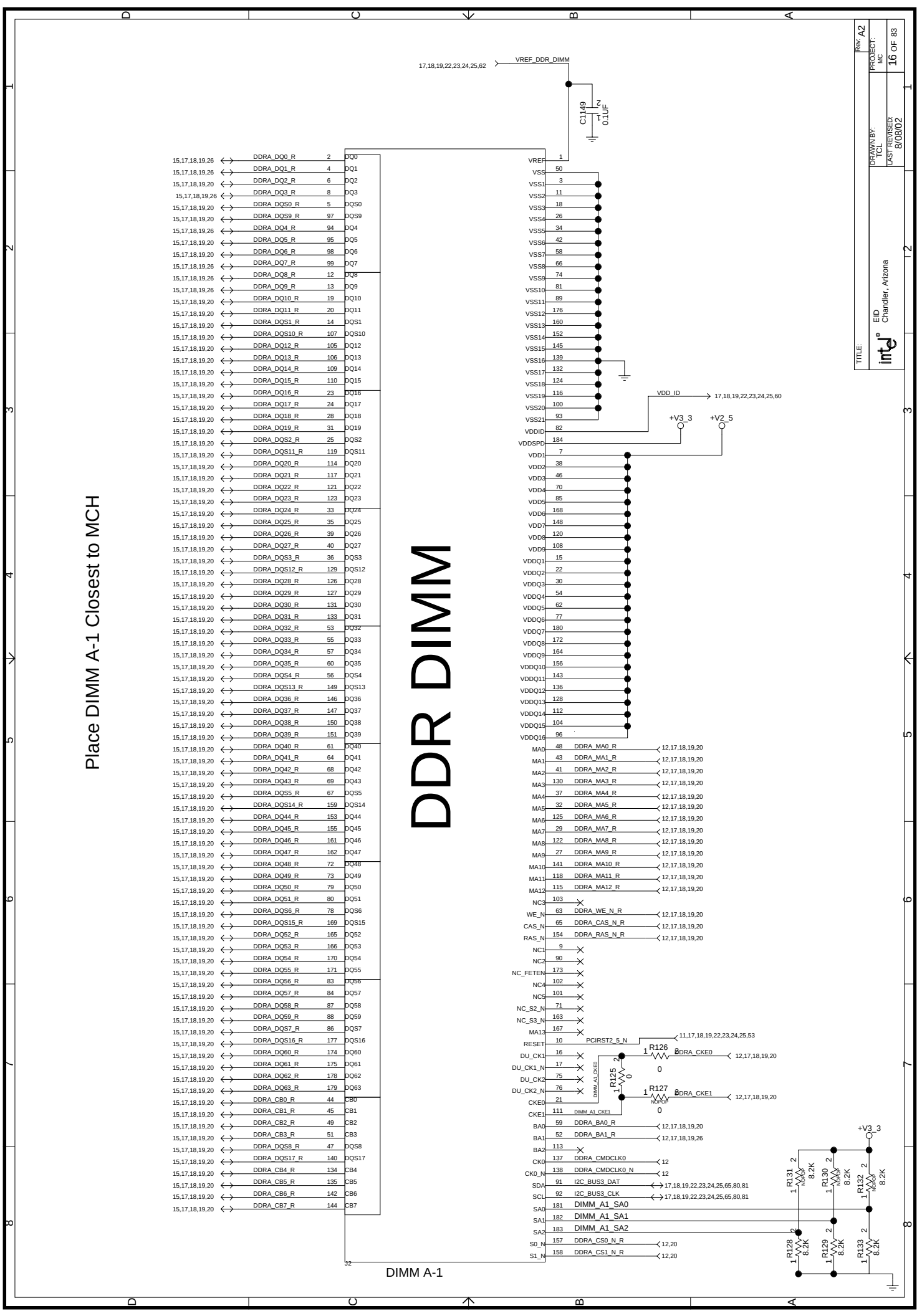
Place DIMM A-1 Closest to MCH
DDR DIMM
DIMM A-1
VREF_DDR_DIMM
17,18,19,22,23,24,25,62
C1149
0.1UF
VDD_ID
17,18,19,22,23,24,25,60
+V3_3
+V2_5
DDRA_CKE0
DDRA_CKE1
PCIRST2_5_N
11,17,18,19,22,23,24,25,53
DIMM_A1_CKE0
DIMM_A1_CKE1
DIMM_A1_SA0
DIMM_A1_SA1
DIMM_A1_SA2
Rev: A2
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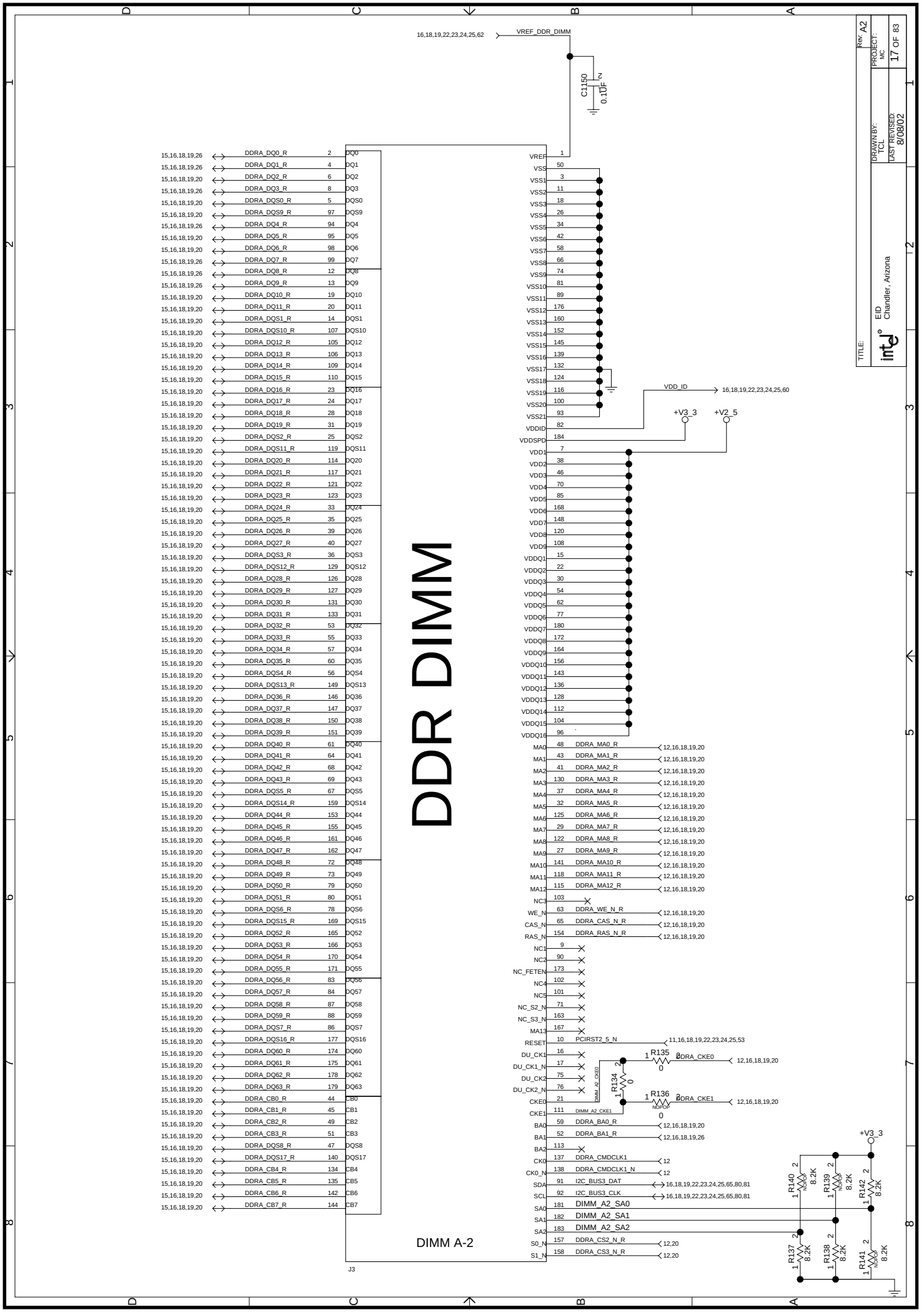
TITLE:
EID
Chandler, Arizona


DDR DIMM
DIMM A-2
VREF_DDR_DIMM
16,18,19,22,23,24,25,62
C1150
0.1UF
VDD_ID
16,18,19,22,23,24,25,60
+V3_3
+V2_5
DDRA_DQ0_R
DDRA_DQ1_R
DDRA_DQ2_R
DDRA_DQ3_R
DDRA_DQS0_R
DDRA_DQS9_R
DDRA_DQ4_R
DDRA_DQ5_R
DDRA_DQ6_R
DDRA_DQ7_R
DDRA_DQ8_R
DDRA_DQ9_R
DDRA_DQ10_R
DDRA_DQ11_R
DDRA_DQS1_R
DDRA_DQS10_R
DDRA_DQ12_R
DDRA_DQ13_R
DDRA_DQ14_R
DDRA_DQ15_R
DDRA_DQ16_R
DDRA_DQ17_R
DDRA_DQ18_R
DDRA_DQ19_R
DDRA_DQS2_R
DDRA_DQS11_R
DDRA_DQ20_R
DDRA_DQ21_R
DDRA_DQ22_R
DDRA_DQ23_R
DDRA_DQ24_R
DDRA_DQ25_R
DDRA_DQ26_R
DDRA_DQ27_R
DDRA_DQS3_R
DDRA_DQS12_R
DDRA_DQ28_R
DDRA_DQ29_R
DDRA_DQ30_R
DDRA_DQ31_R
DDRA_DQ32_R
DDRA_DQ33_R
DDRA_DQ34_R
DDRA_DQ35_R
DDRA_DQS4_R
DDRA_DQS13_R
DDRA_DQ36_R
DDRA_DQ37_R
DDRA_DQ38_R
DDRA_DQ39_R
DDRA_DQ40_R
DDRA_DQ41_R
DDRA_DQ42_R
DDRA_DQ43_R
DDRA_DQS5_R
DDRA_DQS14_R
DDRA_DQ44_R
DDRA_DQ45_R
DDRA_DQ46_R
DDRA_DQ47_R
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DDRA_DQ51_R
DDRA_DQS6_R
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DDRA_DQ59_R
DDRA_DQS7_R
DDRA_DQS16_R
DDRA_DQ60_R
DDRA_DQ61_R
DDRA_DQ62_R
DDRA_DQ63_R
DDRA_CB0_R
DDRA_CB1_R
DDRA_CB2_R
DDRA_CB3_R
DDRA_DQS8_R
DDRA_DQS17_R
DDRA_CB4_R
DDRA_CB5_R
DDRA_CB6_R
DDRA_CB7_R
DDRA_MA0_R
DDRA_MA1_R
DDRA_MA2_R
DDRA_MA3_R
DDRA_MA4_R
DDRA_MA5_R
DDRA_MA6_R
DDRA_MA7_R
DDRA_MA8_R
DDRA_MA9_R
DDRA_MA10_R
DDRA_MA11_R
DDRA_MA12_R
DDRA_WE_N_R
DDRA_CAS_N_R
DDRA_RAS_N_R
PCIRST2_5_N
11,16,18,19,22,23,24,25,53
DDRA_CKE0
DDRA_CKE1
DIMM_A2_CKE0
DIMM_A2_CKE1
DDRA_BA0_R
DDRA_BA1_R
DDRA_CMDCLK1
DDRA_CMDCLK1_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_A2_SA0
DIMM_A2_SA1
DIMM_A2_SA2
DDRA_CS2_N_R
DDRA_CS3_N_R
R135
R136
R134
R140
R139
R142
R137
R138
R141
8.2K
NOPOP
J3
TITLE:
EID
Chandler, Arizona
DRAWN BY:
TCL
LAST REVISED:
8/08/02
PROJECT:
MC
Rev: A2
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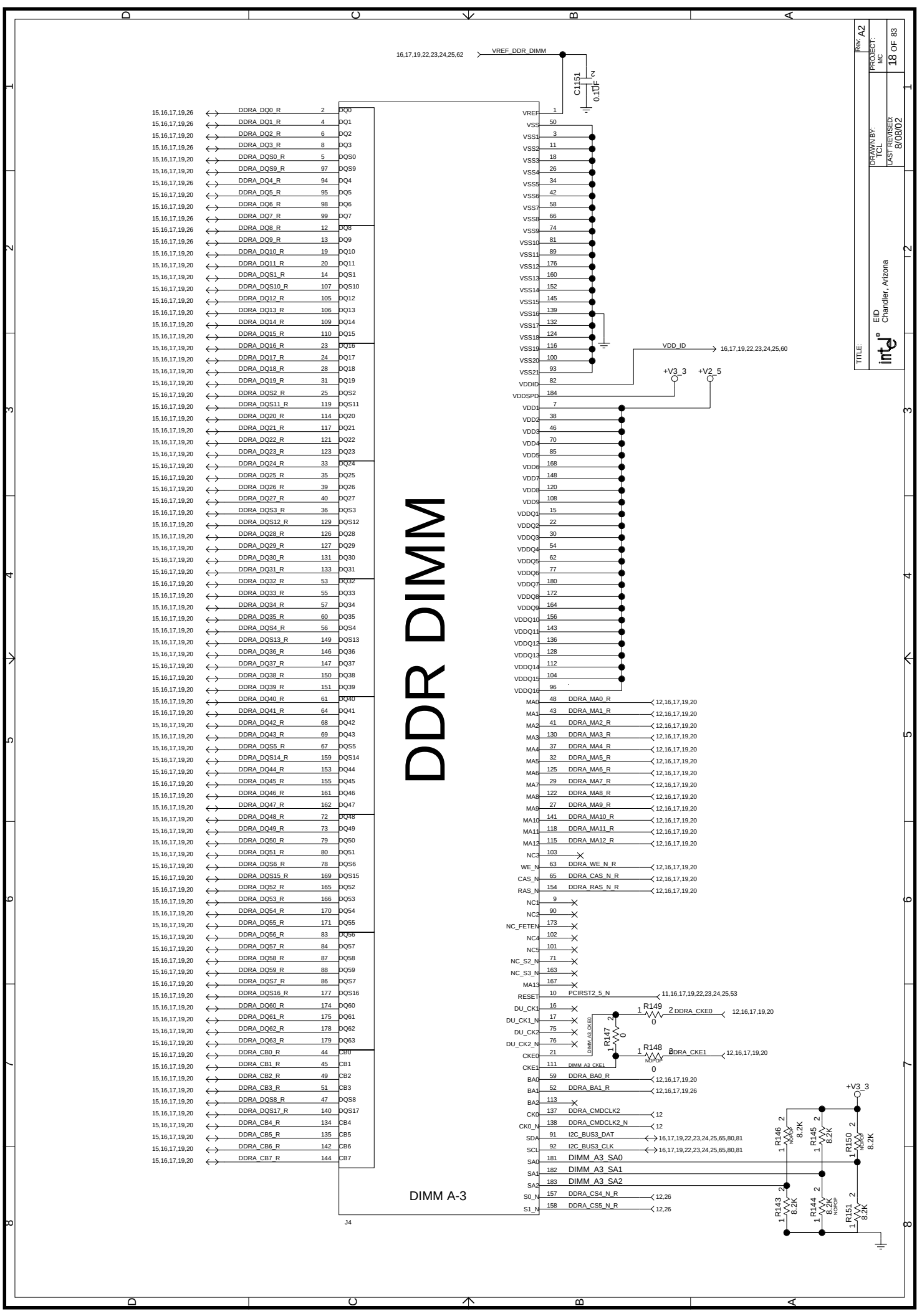
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DIMM A-3
VREF_DDR_DIMM
C1151
0.1UF
VDD_ID
+V3_3
+V2_5
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DDRA_DQ1_R
DDRA_DQ2_R
DDRA_DQ3_R
DDRA_DQS0_R
DDRA_DQS9_R
DDRA_DQ4_R
DDRA_DQ5_R
DDRA_DQ6_R
DDRA_DQ7_R
DDRA_DQ8_R
DDRA_DQ9_R
DDRA_DQ10_R
DDRA_DQ11_R
DDRA_DQS1_R
DDRA_DQS10_R
DDRA_DQ12_R
DDRA_DQ13_R
DDRA_DQ14_R
DDRA_DQ15_R
DDRA_DQ16_R
DDRA_DQ17_R
DDRA_DQ18_R
DDRA_DQ19_R
DDRA_DQS2_R
DDRA_DQS11_R
DDRA_DQ20_R
DDRA_DQ21_R
DDRA_DQ22_R
DDRA_DQ23_R
DDRA_DQ24_R
DDRA_DQ25_R
DDRA_DQ26_R
DDRA_DQ27_R
DDRA_DQS3_R
DDRA_DQS12_R
DDRA_DQ28_R
DDRA_DQ29_R
DDRA_DQ30_R
DDRA_DQ31_R
DDRA_DQ32_R
DDRA_DQ33_R
DDRA_DQ34_R
DDRA_DQ35_R
DDRA_DQS4_R
DDRA_DQS13_R
DDRA_DQ36_R
DDRA_DQ37_R
DDRA_DQ38_R
DDRA_DQ39_R
DDRA_DQ40_R
DDRA_DQ41_R
DDRA_DQ42_R
DDRA_DQ43_R
DDRA_DQS5_R
DDRA_DQS14_R
DDRA_DQ44_R
DDRA_DQ45_R
DDRA_DQ46_R
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DDRA_DQ51_R
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DDRA_DQS15_R
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DDRA_DQ53_R
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DDRA_DQ57_R
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DDRA_DQ59_R
DDRA_DQS7_R
DDRA_DQS16_R
DDRA_DQ60_R
DDRA_DQ61_R
DDRA_DQ62_R
DDRA_DQ63_R
DDRA_CB0_R
DDRA_CB1_R
DDRA_CB2_R
DDRA_CB3_R
DDRA_DQS8_R
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DDRA_CB4_R
DDRA_CB5_R
DDRA_CB6_R
DDRA_CB7_R
DDRA_MA0_R
DDRA_MA1_R
DDRA_MA2_R
DDRA_MA3_R
DDRA_MA4_R
DDRA_MA5_R
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DDRA_MA7_R
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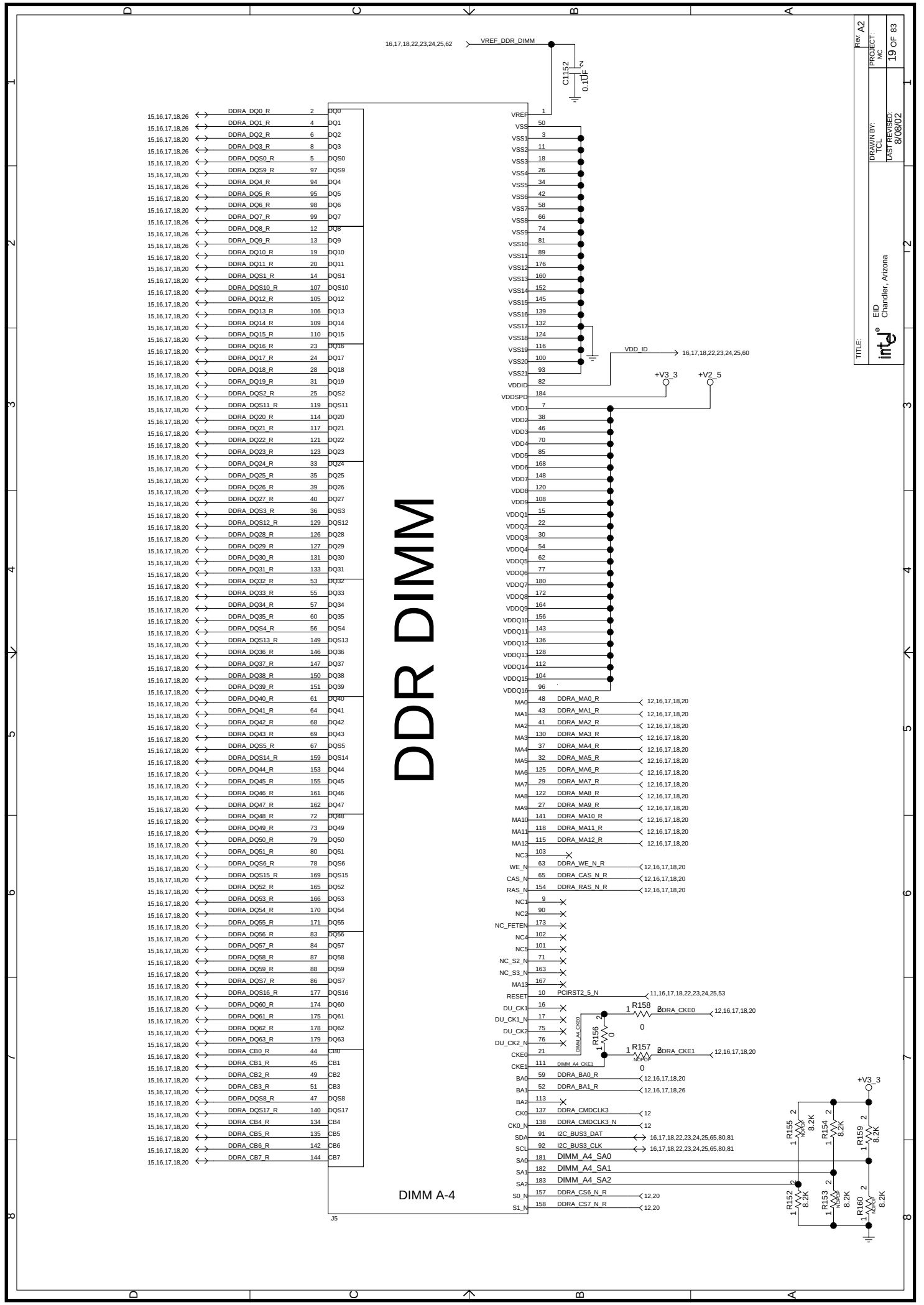
DDRA_MA11_R
DDRA_MA12_R
DDRA_WE_N_R
DDRA_CAS_N_R
DDRA_RAS_N_R
PCIRST2_5_N
DDRA_CKE0
DDRA_CKE1
DDRA_BA0_R
DDRA_BA1_R
DDRA_CMDCLK2
DDRA_CMDCLK2_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_A3_SA0
DIMM_A3_SA1
DIMM_A3_SA2
DDRA_CS4_N_R
DDRA_CS5_N_R
R149
R147
R148
R146
R145
R150
R143
R144
R151
8.2K
NOPOP
J4
TITLE:
intel
EID
Chandler, Arizona
DRAWN BY:
TCL
LAST REVISED:
8/08/02
PROJECT:
MC
18 OF 83
Rev: A2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DIMM A-4
VREF_DDR_DIMM
C1152
0.1UF
VDD_ID
+V3_3
+V2_5
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DDRA_DQ1_R
DDRA_DQ2_R
DDRA_DQ3_R
DDRA_DQS0_R
DDRA_DQS9_R
DDRA_DQ4_R
DDRA_DQ5_R
DDRA_DQ6_R
DDRA_DQ7_R
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DDRA_DQ9_R
DDRA_DQ10_R
DDRA_DQ11_R
DDRA_DQS1_R
DDRA_DQS10_R
DDRA_DQ12_R
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DDRA_DQ14_R
DDRA_DQ15_R
DDRA_DQ16_R
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DDRA_DQ18_R
DDRA_DQ19_R
DDRA_DQS2_R
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DDRA_DQ25_R
DDRA_DQ26_R
DDRA_DQ27_R
DDRA_DQS3_R
DDRA_DQS12_R
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DDRA_DQS5_R
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DDRA_DQS16_R
DDRA_DQ60_R
DDRA_DQ61_R
DDRA_DQ62_R
DDRA_DQ63_R
DDRA_CB0_R
DDRA_CB1_R
DDRA_CB2_R
DDRA_CB3_R
DDRA_DQS8_R
DDRA_DQS17_R
DDRA_CB4_R
DDRA_CB5_R
DDRA_CB6_R
DDRA_CB7_R
DDRA_MA0_R
DDRA_MA1_R
DDRA_MA2_R
DDRA_MA3_R
DDRA_MA4_R
DDRA_MA5_R
DDRA_MA6_R
DDRA_MA7_R
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DDRA_MA11_R
DDRA_MA12_R
DDRA_WE_N_R
DDRA_CAS_N_R
DDRA_RAS_N_R
PCIRST2_5_N
R158
R156
R157
DDRA_CKE0
DDRA_CKE1
DIMM_A4_CKE0
DIMM_A4_CKE1
DDRA_BA0_R
DDRA_BA1_R
DDRA_CMDCLK3
DDRA_CMDCLK3_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_A4_SA0
DIMM_A4_SA1
DIMM_A4_SA2
DDRA_CS6_N_R
DDRA_CS7_N_R
R155
R154
R159
R152
R153
R160
8.2K
J5
TITLE:
intel
EID
Chandler, Arizona
DRAWN BY:
TCL
LAST REVISED:
8/08/02
PROJECT:
MC
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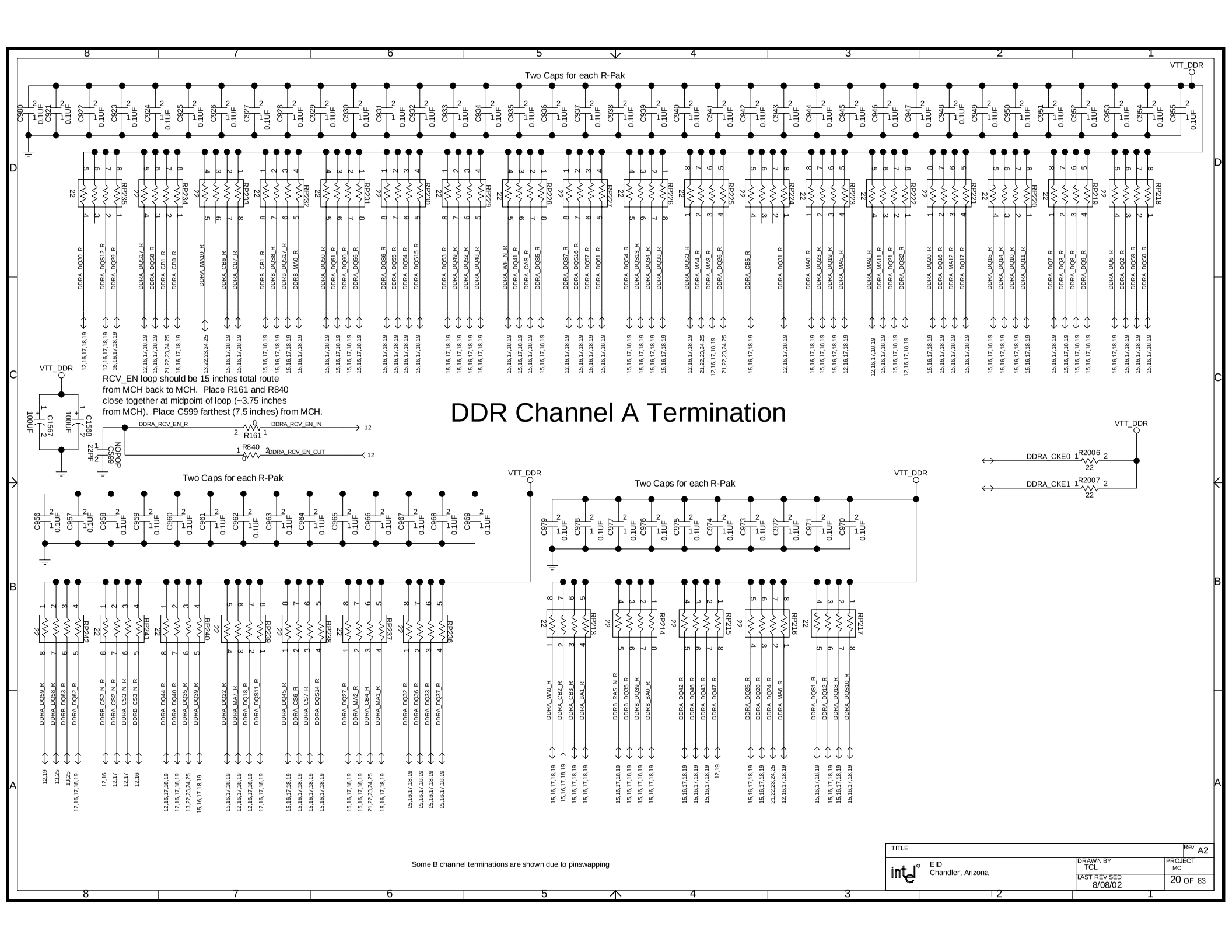
Rev: A2

DDR Channel A Termination



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intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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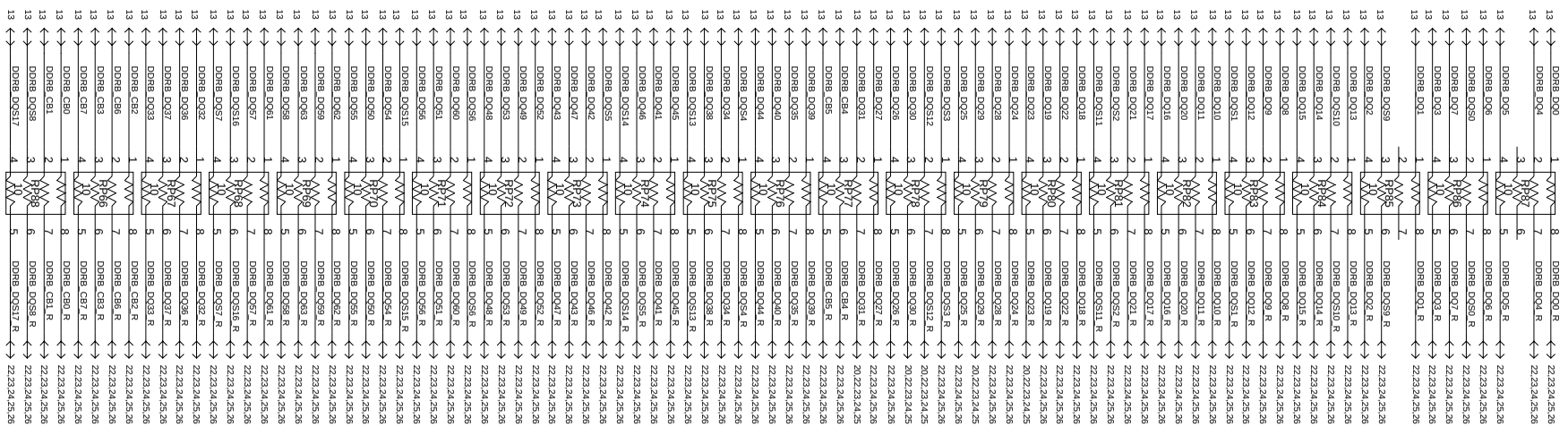
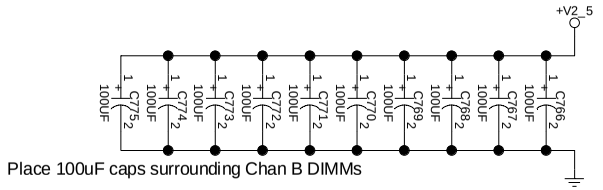
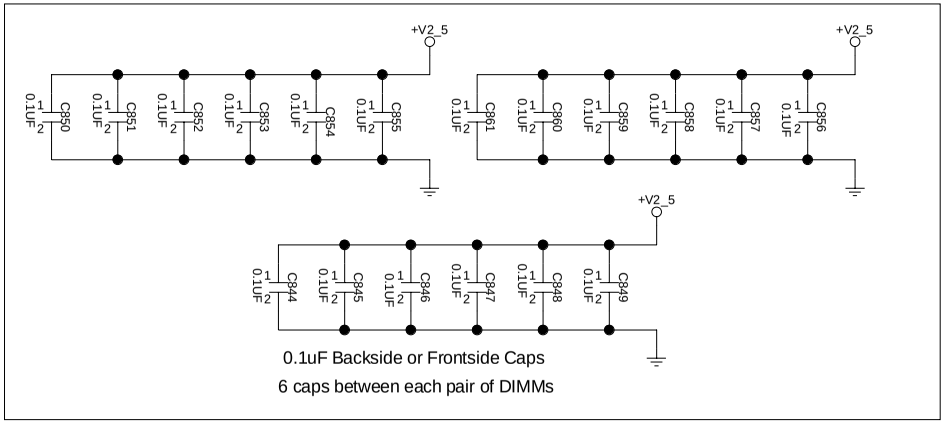
DDR Channel B Series Resistors

Place near DIMM B-1





Place 100uF caps surrounding Chan B DIMMs



0.1uF Backside or Frontside Caps

6 caps between each pair of DIMMs

CAD Note: All Caps should have direct attatchment to 2.5V plane, and 2 vias to GND.

TITLE:		Rev: A2
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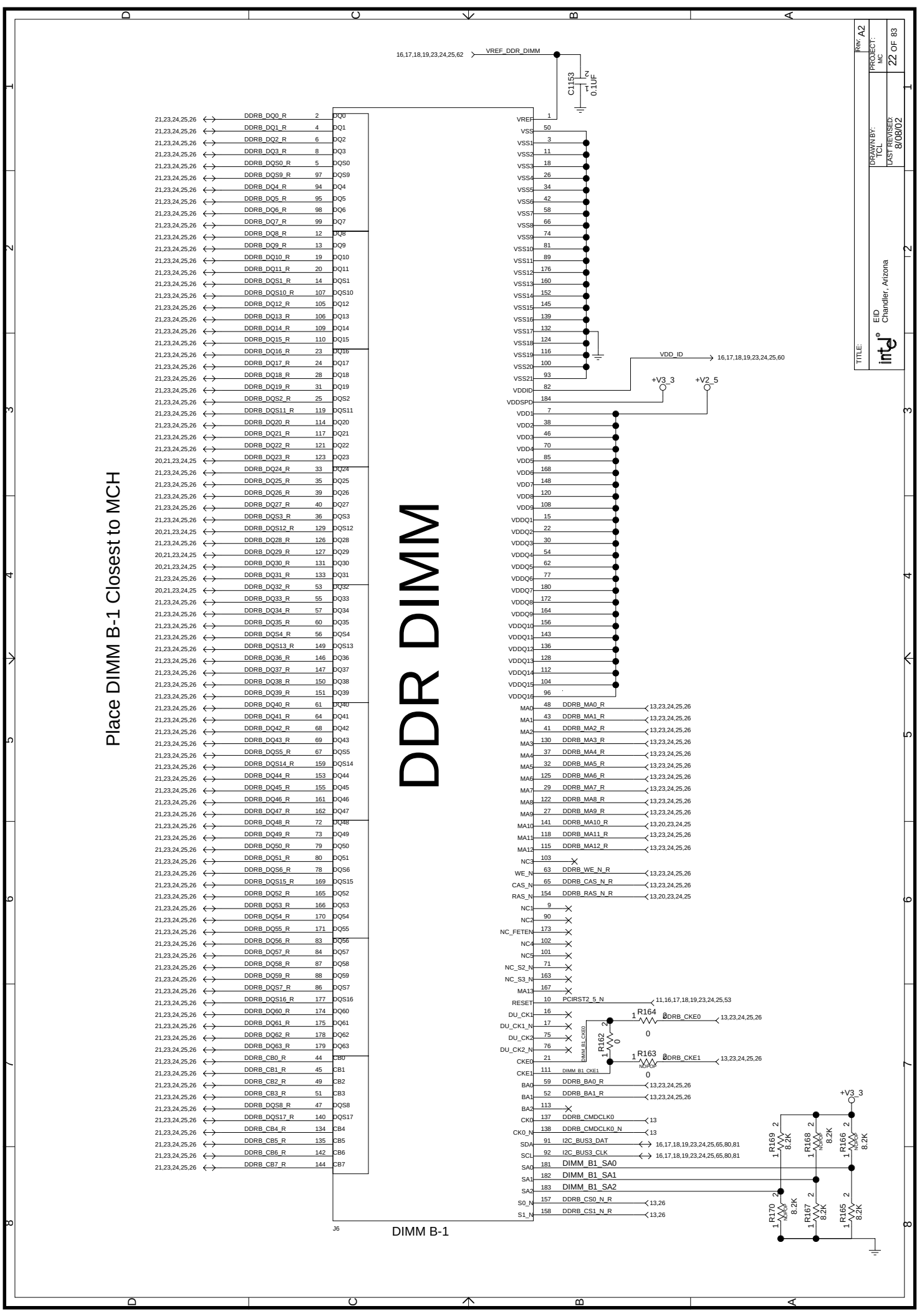
Place DIMM B-1 Closest to MCH
DDR DIMM
DIMM B-1
J6
VREF_DDR_DIMM
C1153
0.1UF
VDD_ID
+V3_3
+V2_5
DDRB_DQ0_R
DDRB_DQ1_R
DDRB_DQ2_R
DDRB_DQ3_R
DDRB_DQS0_R
DDRB_DQS9_R
DDRB_DQ4_R
DDRB_DQ5_R
DDRB_DQ6_R
DDRB_DQ7_R
DDRB_DQ8_R
DDRB_DQ9_R
DDRB_DQ10_R
DDRB_DQ11_R
DDRB_DQS1_R
DDRB_DQS10_R
DDRB_DQ12_R
DDRB_DQ13_R
DDRB_DQ14_R
DDRB_DQ15_R
DDRB_DQ16_R
DDRB_DQ17_R
DDRB_DQ18_R
DDRB_DQ19_R
DDRB_DQS2_R
DDRB_DQS11_R
DDRB_DQ20_R
DDRB_DQ21_R
DDRB_DQ22_R
DDRB_DQ23_R
DDRB_DQ24_R
DDRB_DQ25_R
DDRB_DQ26_R
DDRB_DQ27_R
DDRB_DQS3_R
DDRB_DQS12_R
DDRB_DQ28_R
DDRB_DQ29_R
DDRB_DQ30_R
DDRB_DQ31_R
DDRB_DQ32_R
DDRB_DQ33_R
DDRB_DQ34_R
DDRB_DQ35_R
DDRB_DQS4_R
DDRB_DQS13_R
DDRB_DQ36_R
DDRB_DQ37_R
DDRB_DQ38_R
DDRB_DQ39_R
DDRB_DQ40_R
DDRB_DQ41_R
DDRB_DQ42_R
DDRB_DQ43_R
DDRB_DQS5_R
DDRB_DQS14_R
DDRB_DQ44_R
DDRB_DQ45_R
DDRB_DQ46_R
DDRB_DQ47_R
DDRB_DQ48_R
DDRB_DQ49_R
DDRB_DQ50_R
DDRB_DQ51_R
DDRB_DQS6_R
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DDRB_DQ52_R
DDRB_DQ53_R
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DDRB_DQ56_R
DDRB_DQ57_R
DDRB_DQ58_R
DDRB_DQ59_R
DDRB_DQS7_R
DDRB_DQS16_R
DDRB_DQ60_R
DDRB_DQ61_R
DDRB_DQ62_R
DDRB_DQ63_R
DDRB_CB0_R
DDRB_CB1_R
DDRB_CB2_R
DDRB_CB3_R
DDRB_DQS8_R
DDRB_DQS17_R
DDRB_CB4_R
DDRB_CB5_R
DDRB_CB6_R
DDRB_CB7_R
DDRB_MA0_R
DDRB_MA1_R
DDRB_MA2_R
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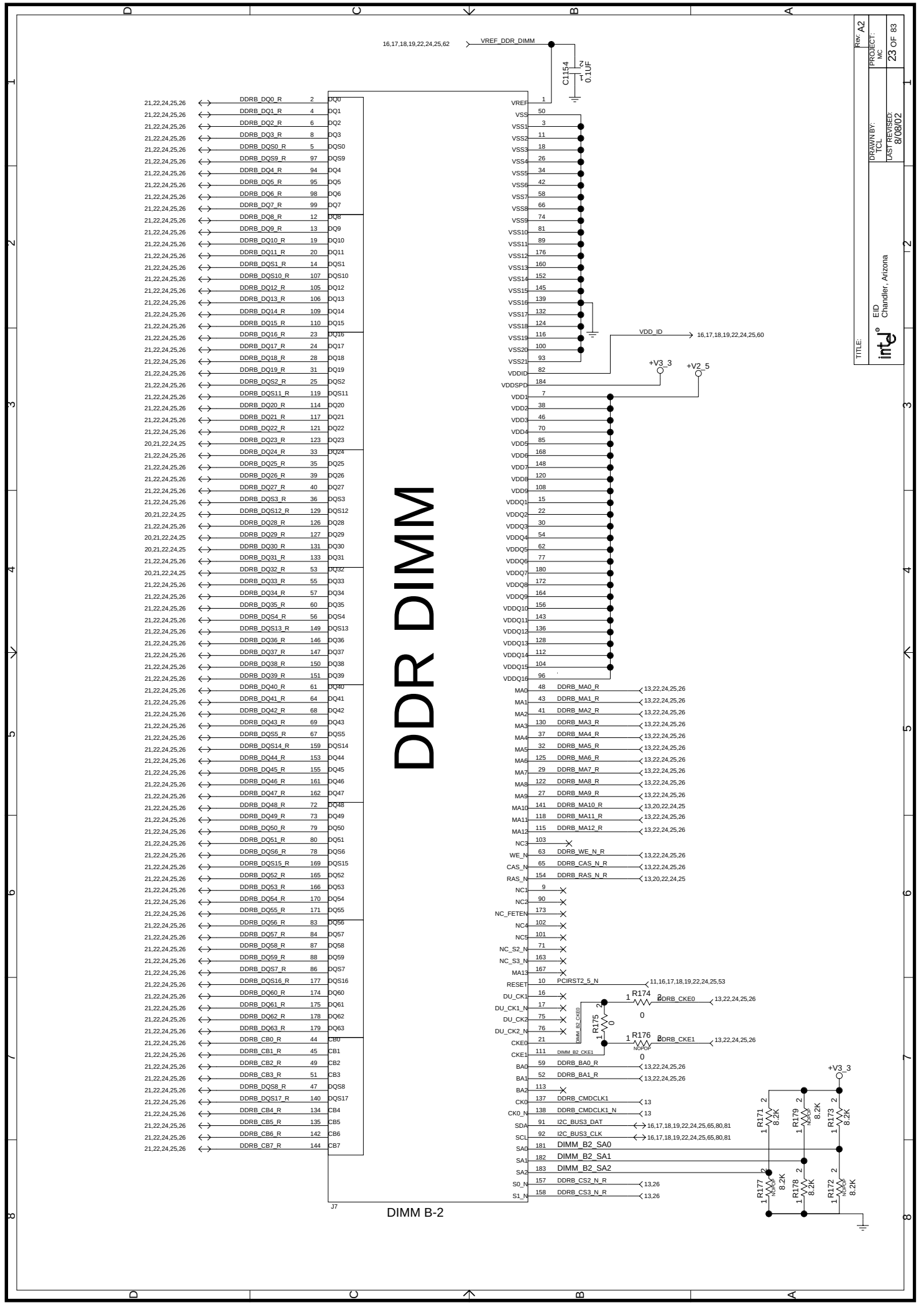
DDRB_MA11_R
DDRB_MA12_R
DDRB_WE_N_R
DDRB_CAS_N_R
DDRB_RAS_N_R
PCIRST2_5_N
DIMM_B1_CKE0
DIMM_B1_CKE1
DDRB_BA0_R
DDRB_BA1_R
DDRB_CMDCLK0
DDRB_CMDCLK0_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_B1_SA0
DIMM_B1_SA1
DIMM_B1_SA2
DDRB_CS0_N_R
DDRB_CS1_N_R
R164
R163
R162
R169
R168
R166
R170
R167
R165
8.2K
0
NOPOP
DRAWN BY: TCL
LAST REVISED: 8/08/02
PROJECT: MC
Rev: A2
22 OF 83
TITLE:
EID
Chandler, Arizona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C1154
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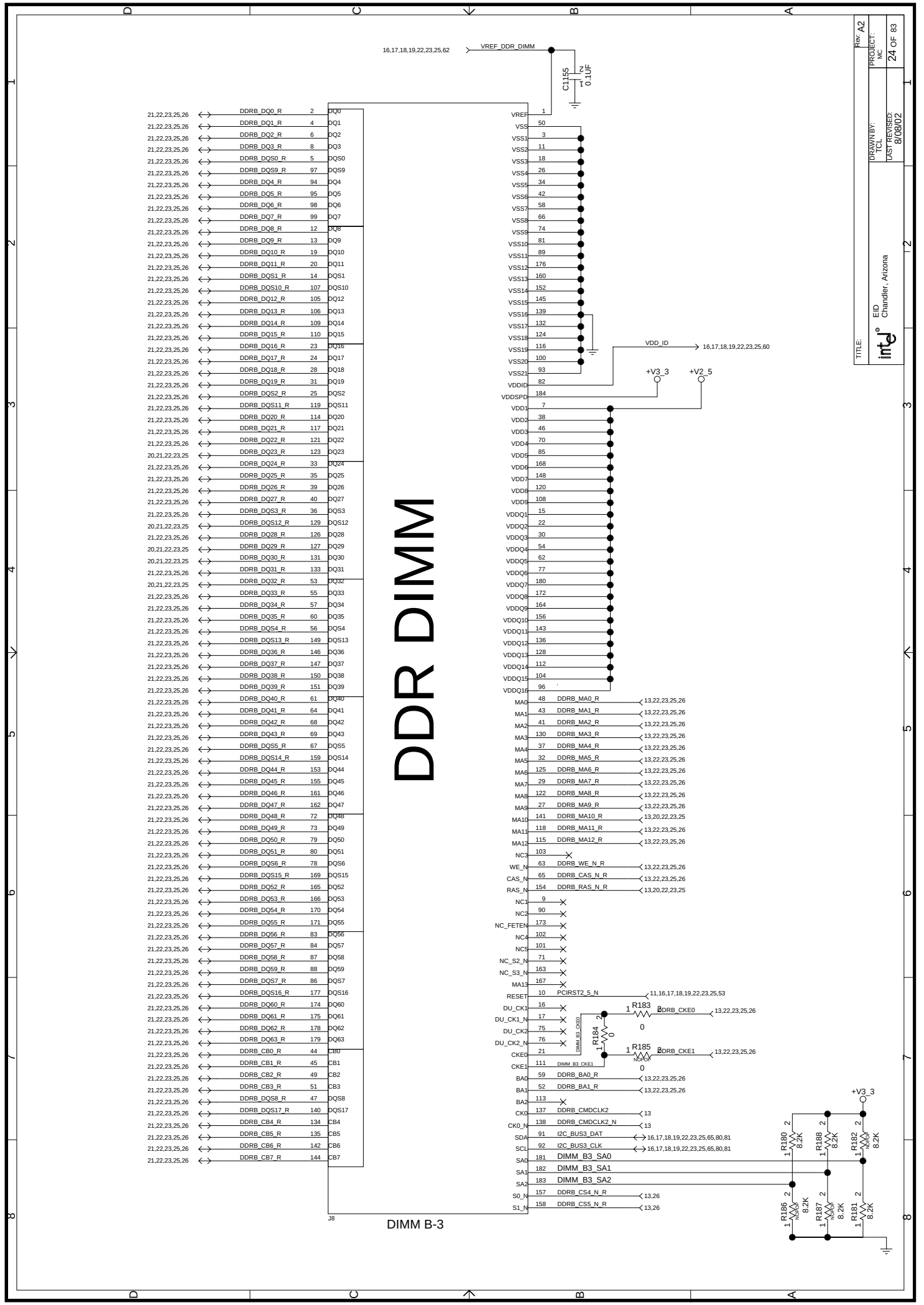
VDD_ID
16,17,18,19,22,24,25,60
+V3_3
+V2_5
DIMM_B2_SA0
DIMM_B2_SA1
DIMM_B2_SA2
DIMM B-2
J7
Rev: A2
PROJECT: MC
23 OF 83
DRAWN BY: TCL
LAST REVISED: 8/08/02
TITLE:
EID
Chandler, Arizona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C1155
0.1UF
VDD_ID
16,17,18,19,22,23,25,60
+V3_3
+V2_5
DIMM_B3_SA0
DIMM_B3_SA1
DIMM_B3_SA2
R180
R188
R182
R186
R187
R181
8.2K
R183
R184
R185
0
DIMM_B3_CKE0
DIMM_B3_CKE1
J8
DIMM B-3
TITLE:
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Chandler, Arizona
DRAWN BY:
TCL
LAST REVISED:
8/08/02
PROJECT:
MC
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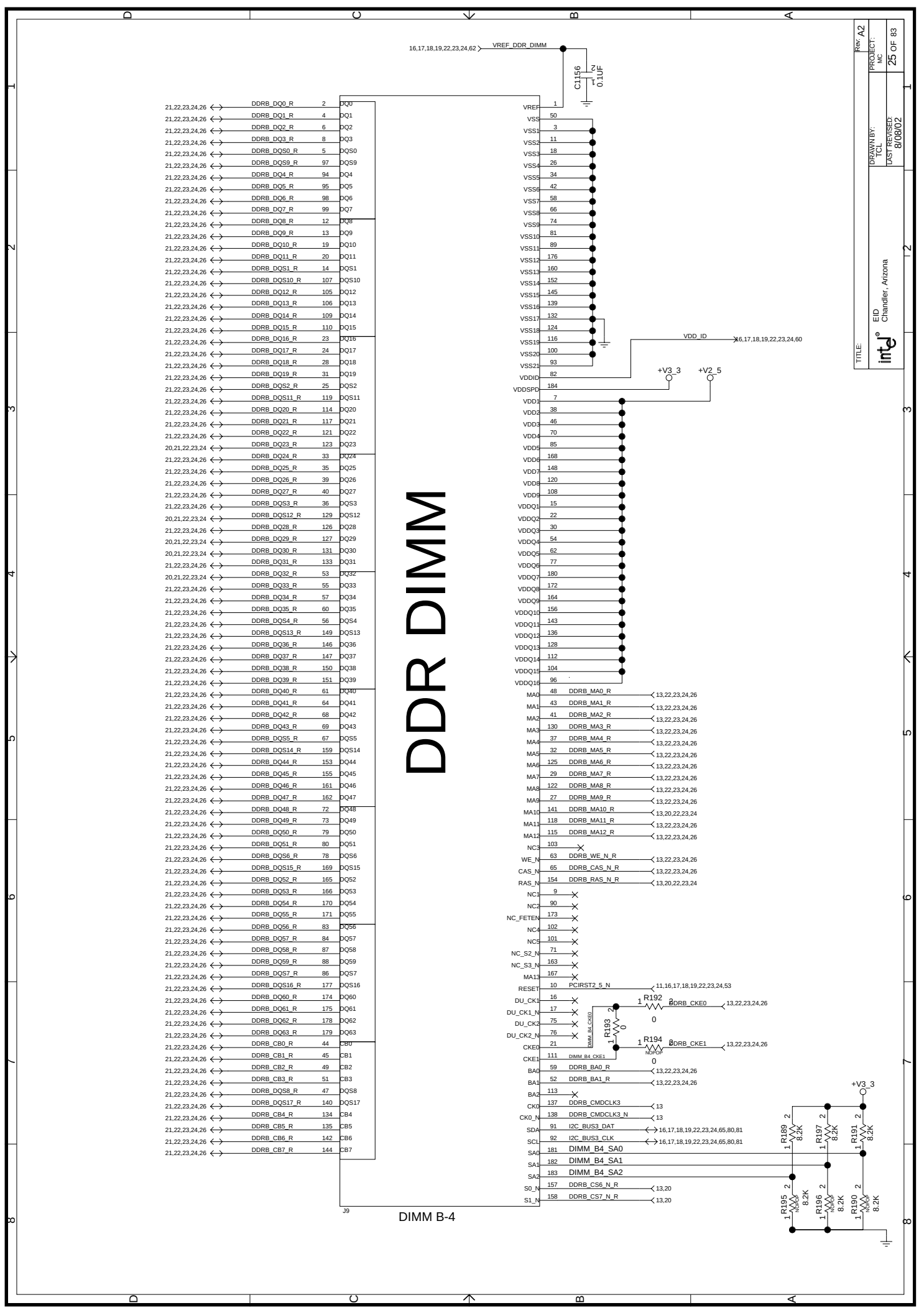
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VDD_ID
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+V2_5
J9
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R192
R193
R194
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DIMM_B4_CKE1
DIMM_B4_SA0
DIMM_B4_SA1
DIMM_B4_SA2
R189
R197
R191
R195
R196
R190
8.2K
NOSTUFF
Rev: A2
PROJECT: MC
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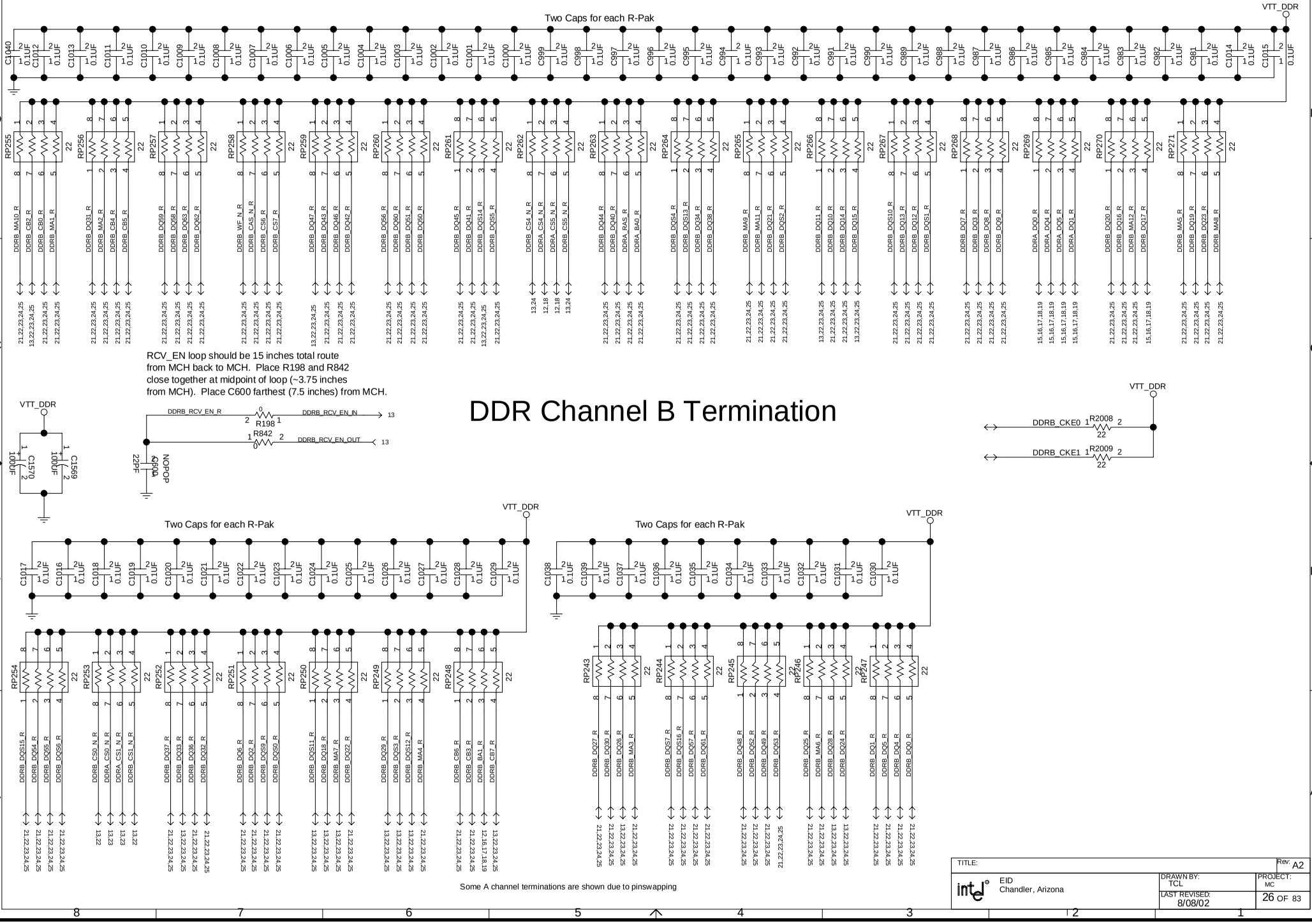
DRAWN BY: TCL
LAST REVISED: 8/08/02
TITLE:
EID
Chandler, Arizona

DDR Channel B Termination



TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
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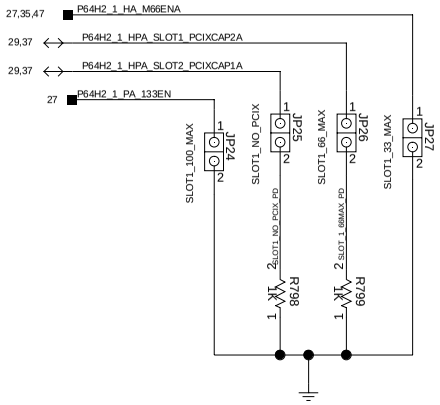
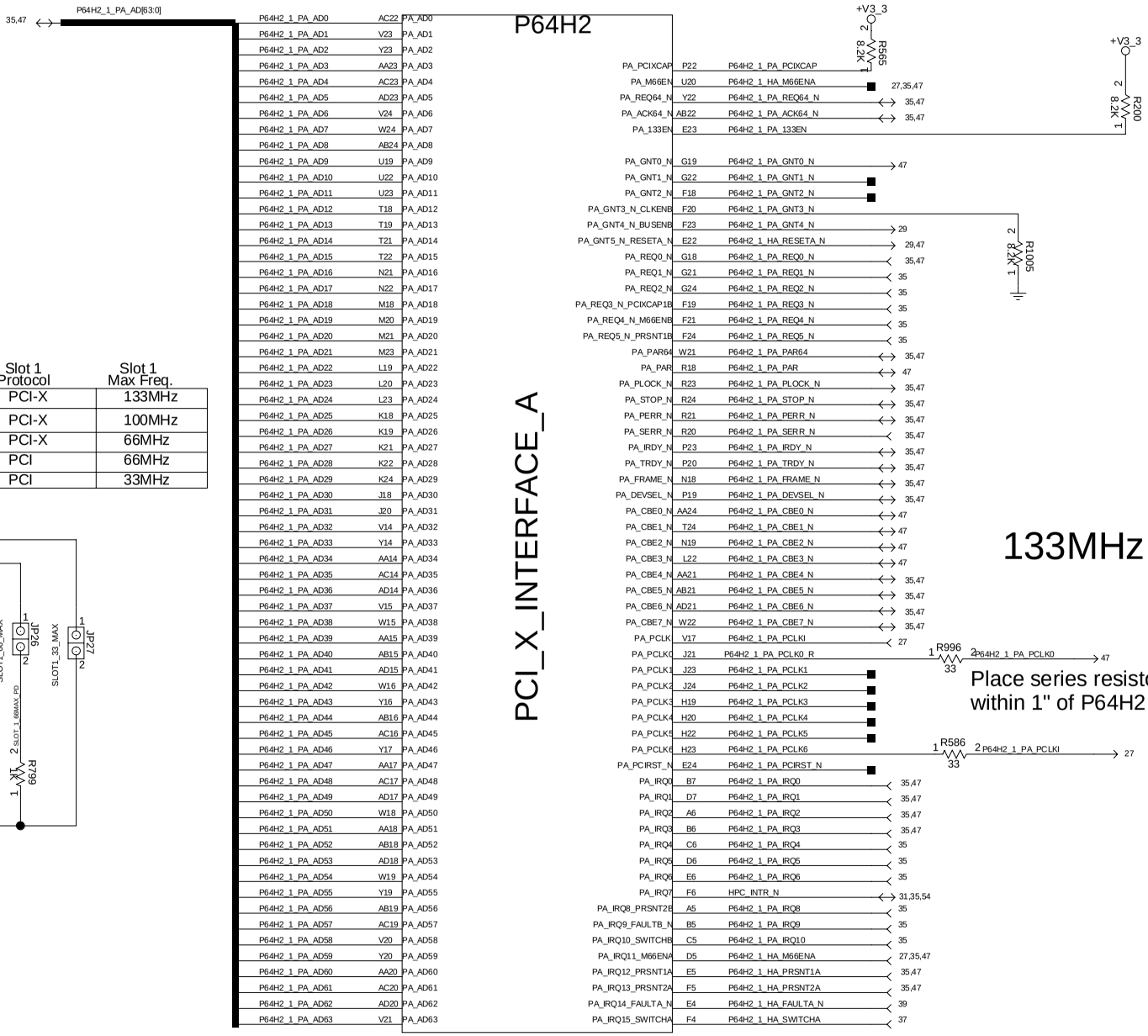
For Validation Only

JP24	JP25	JP26	JP27	Slot 1 Protocol	Slot 1 Max Freq.
No Jumper	No Jumper	No Jumper	No Jumper	PCI-X	133MHz
Jumper	No Jumper	No Jumper	No Jumper	PCI-X	100MHz
Jumper	No Jumper	Jumper	No Jumper	PCI-X	66MHz
Jumper	Jumper	Jumper	No Jumper	PCI	66MHz
Jumper	Jumper	Jumper	Jumper	PCI	33MHz





133MHz Slot 1

P64H2 #1

TITLE:	Rev: A2
EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
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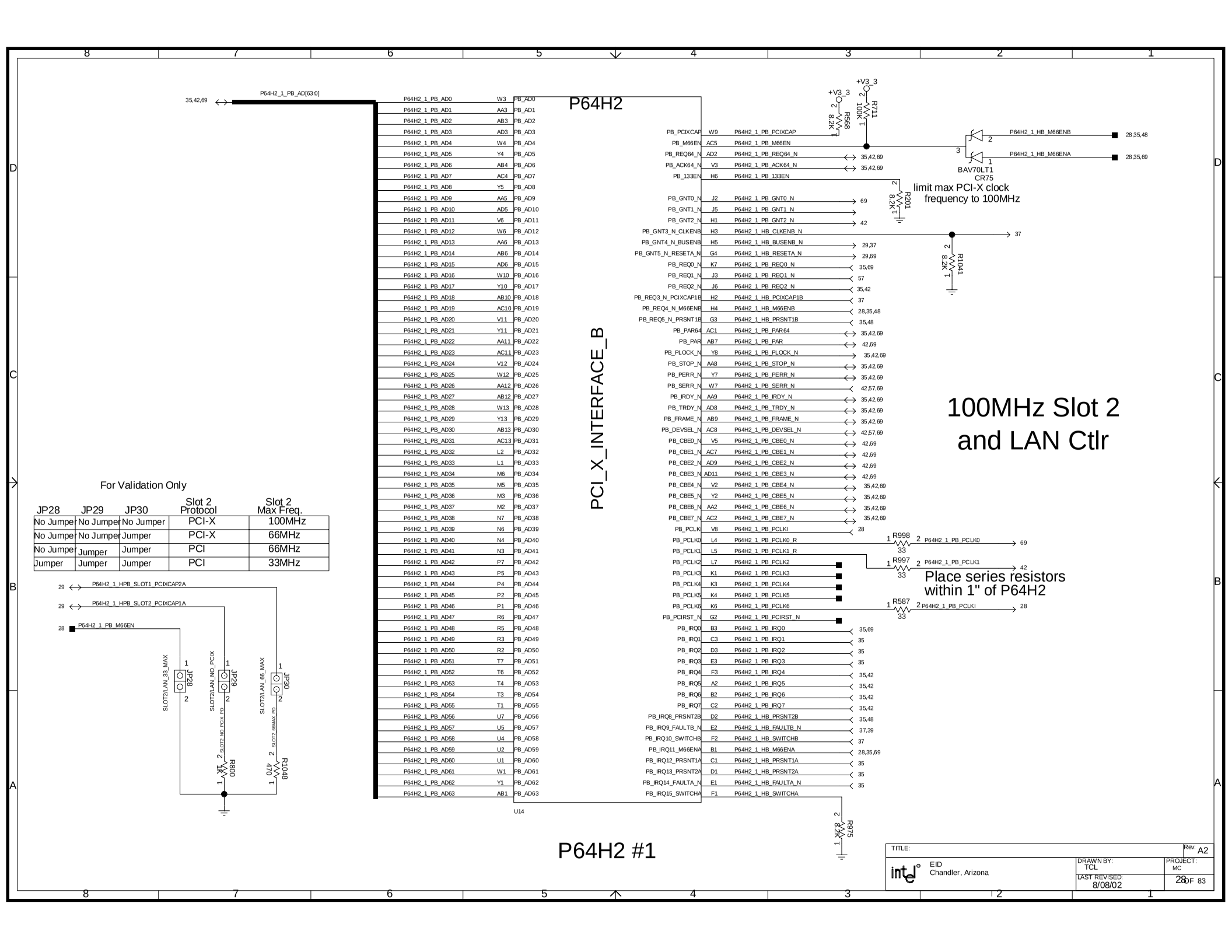
P64H2
PCI_X_INTERFACE_B
100MHz Slot 2
and LAN Ctlr
P64H2 #1
For Validation Only
JP28 JP29 JP30 Slot 2 Protocol Slot 2 Max Freq.
No Jumper No Jumper No Jumper PCI-X 100MHz
No Jumper No Jumper Jumper PCI-X 66MHz
No Jumper Jumper Jumper PCI 66MHz
Jumper Jumper Jumper PCI 33MHz
limit max PCI-X clock frequency to 100MHz
Place series resistors within 1" of P64H2
BAV70LT1
CR75
U14
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
LAST REVISED: 8/08/02
PROJECT: MC
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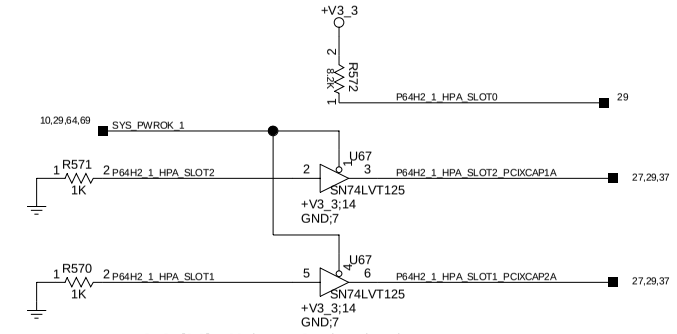
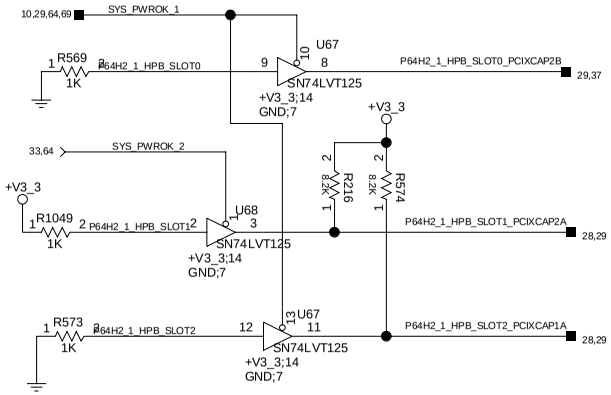
P64H2 #1

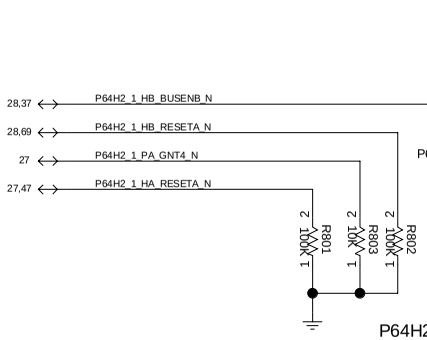


HPA_SLOT[2:0] = 001b ==> One hot-plug slot



HPB_SLOT[2:0] = 010b ==> Two hot-plug slots

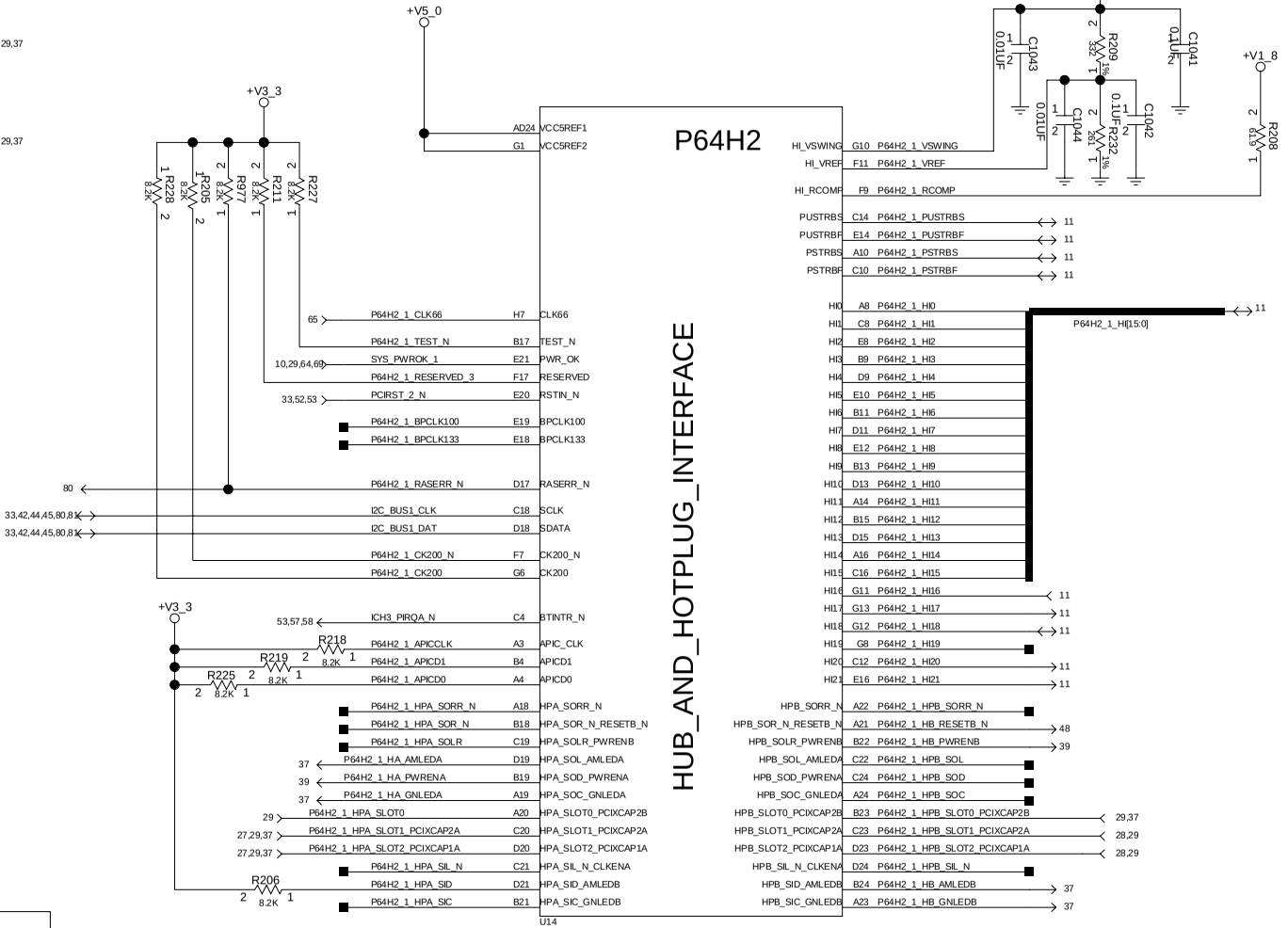
PCIXCAP[2:1]B= 11b ==> 100MHz PCI-X capable



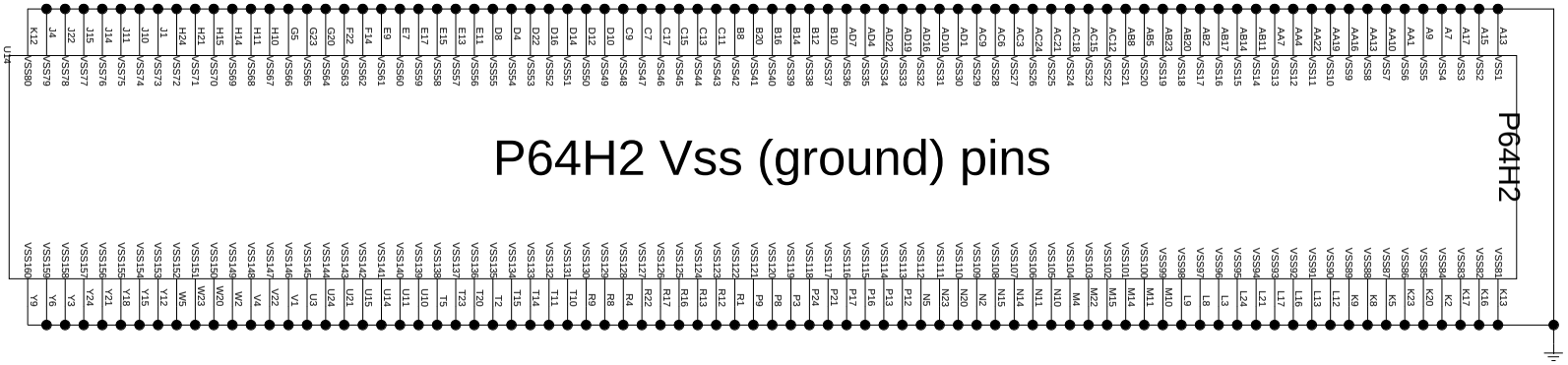
P64H2 SMBus Address Strapping

Bit	Value
7	1
6	1
5	PA_GNT5_RESETA_N
4	0
3	PA_GNT4_BUSENB_N
2	PB_GNT5_RESETA_N
1	PB_GNT4_BUSENB_N

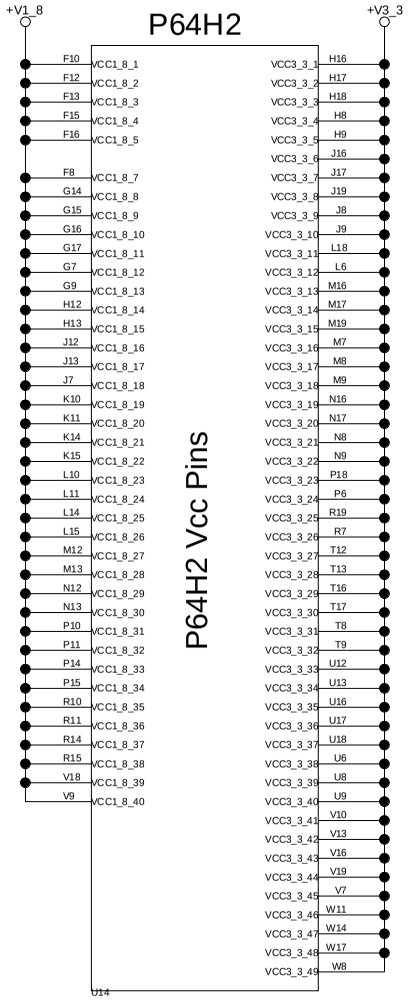
P64H2 #1 SMBus Address = C2h

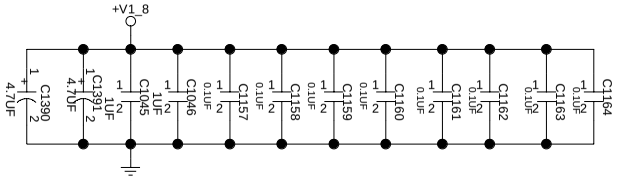


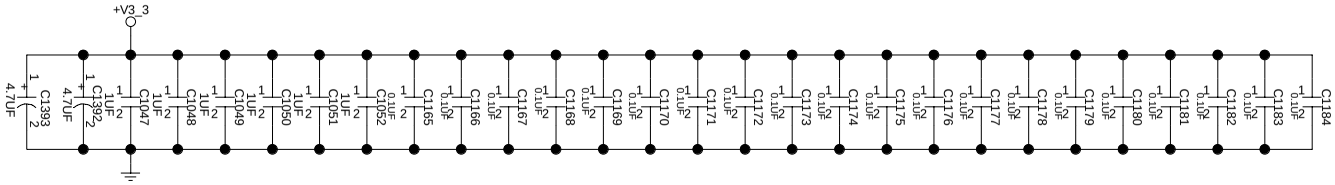
TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	29 OF 83	



P64H2 Vss (ground) pins







P64H2 #1 power, ground and decoupling

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	30 OF 83

133MHz AIC-7902 SCSI

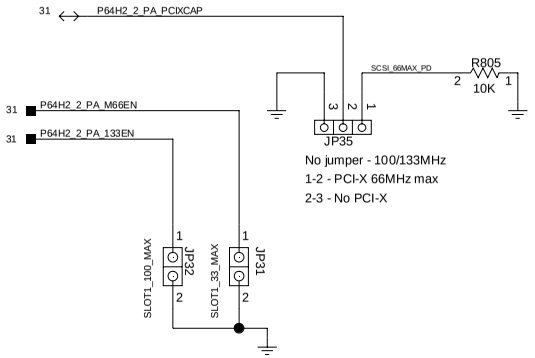
P64H2

PCI_X_INTERFACE_A

P64H2 #2

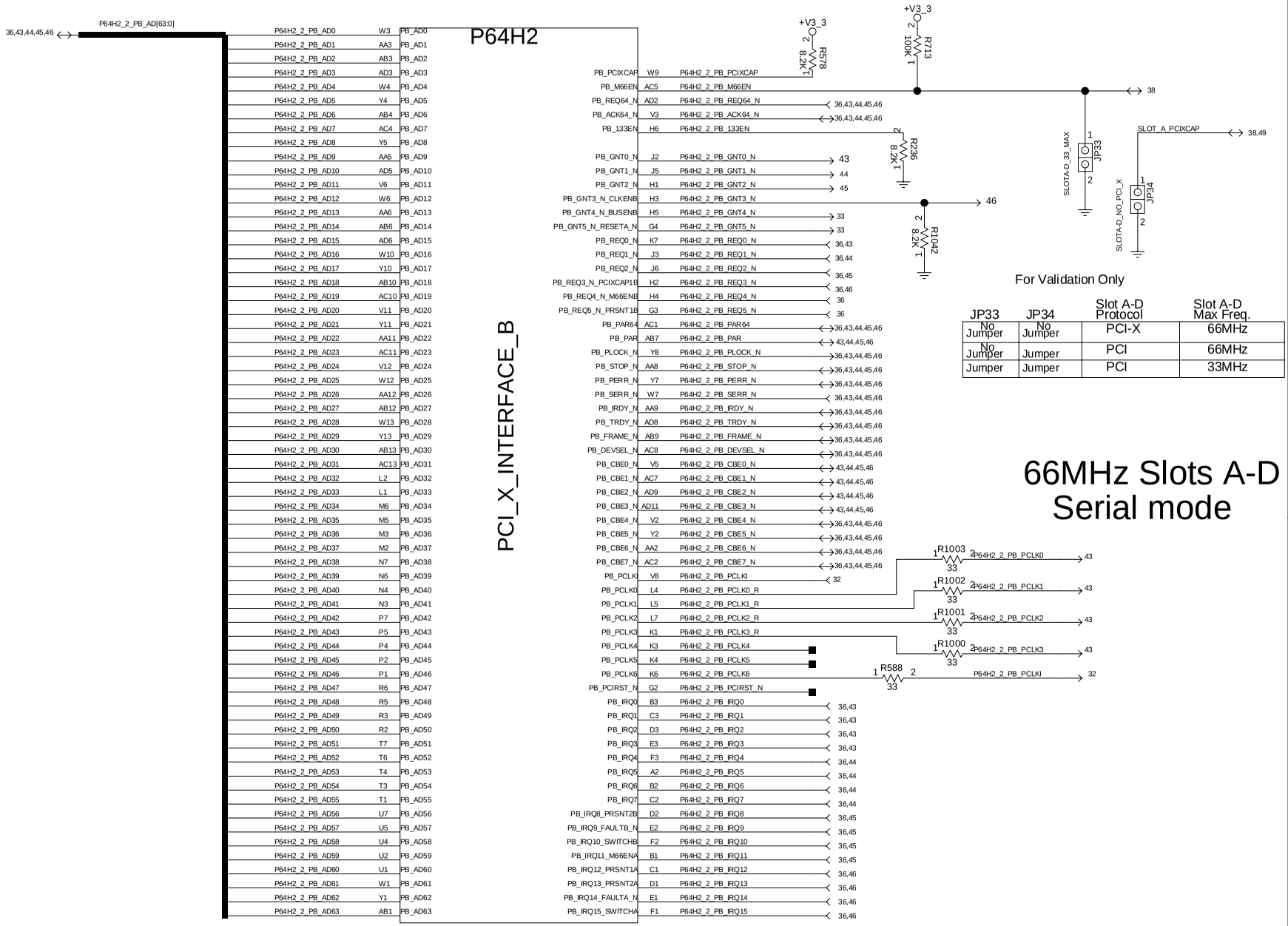
For Validation Only

JP31	JP32	JP35	Protocol	Max Freq.
No Jumper	No Jumper	No Jumper	PCI-X	133MHz
No Jumper	Jumper	No Jumper	PCI-X	100MHz
No Jumper	Jumper	Pin 1-2	PCI-X	66MHz
No Jumper	Jumper	Pin 2-3	PCI	66MHz
Jumper	Jumper	Pin 2-3	PCI	33MHz



Place series resistors within 1" of P64H2

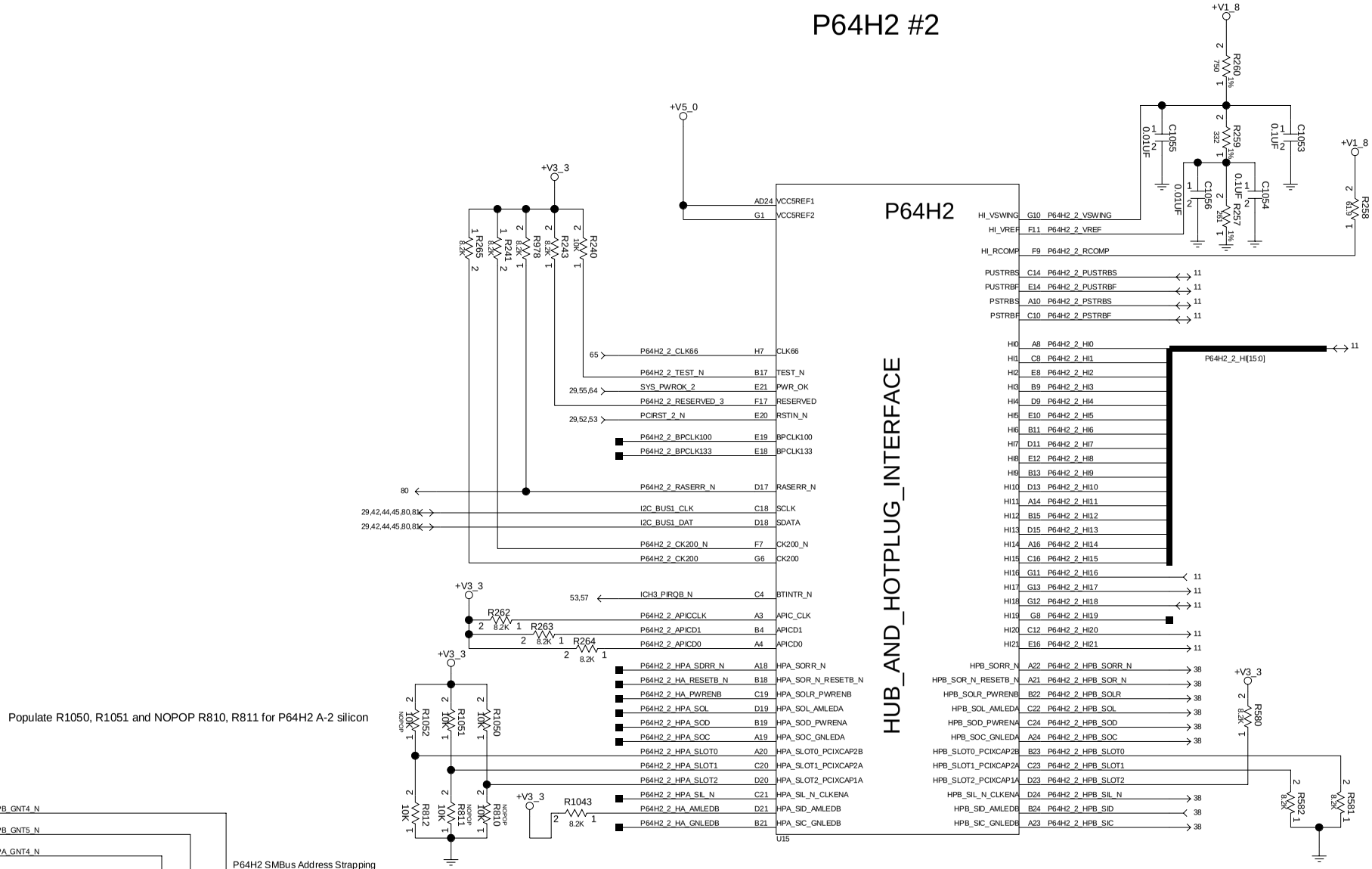
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	31 OF 83



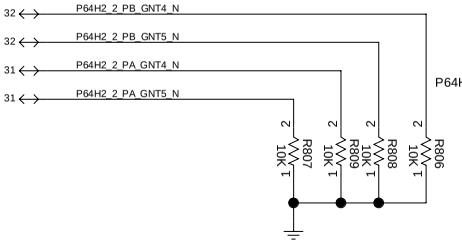
P64H2 #2

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	32 OF 83

P64H2 #2



Populate R1050, R1051 and NOPOP R810, R811 for P64H2 A-2 silicon

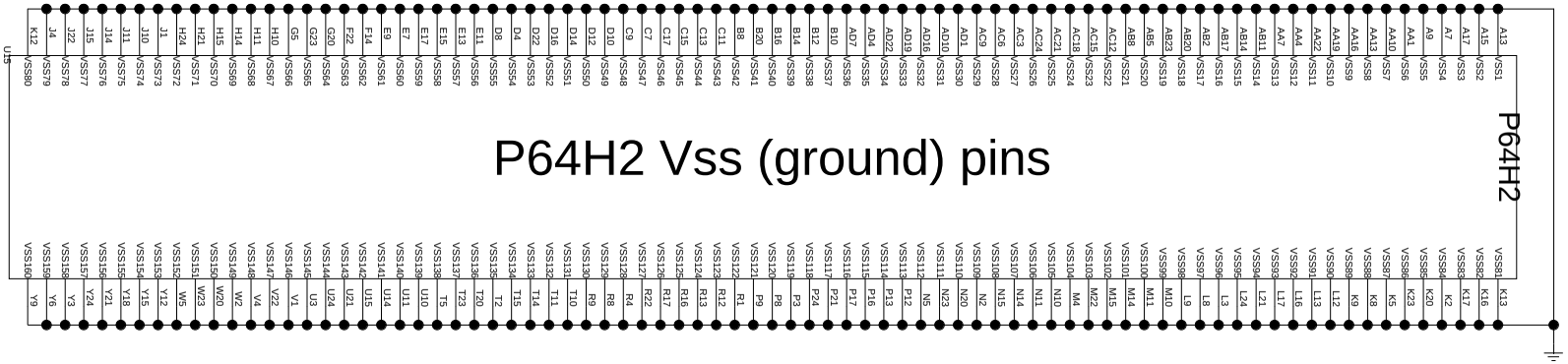


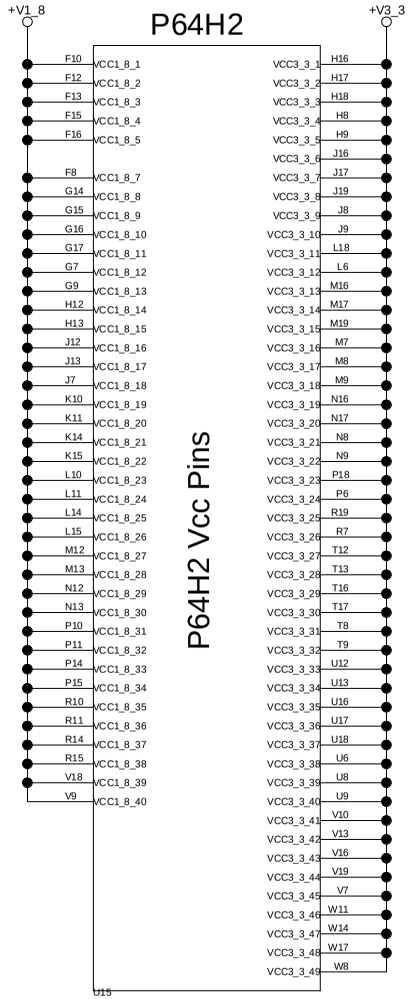
P64H2 SMBus Address Strapping

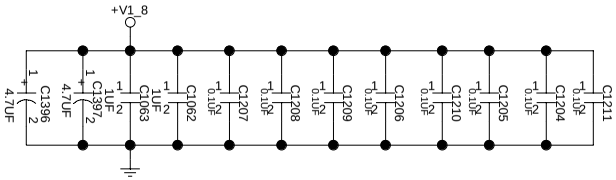
Bit	Value
7	1
6	1
5	PA_GNT5_RESETA_N
4	0
3	PA_GNT4_BUSENB_N
2	PB_GNT5_RESETA_N
1	PB_GNT4_BUSENB_N

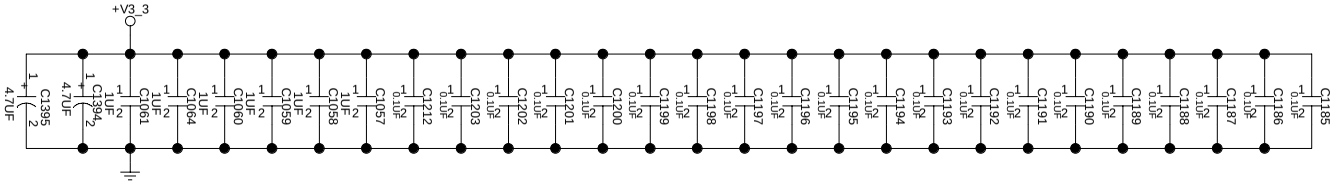
P64H2 #2 SMBus Address = C0h

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	33 OF 83



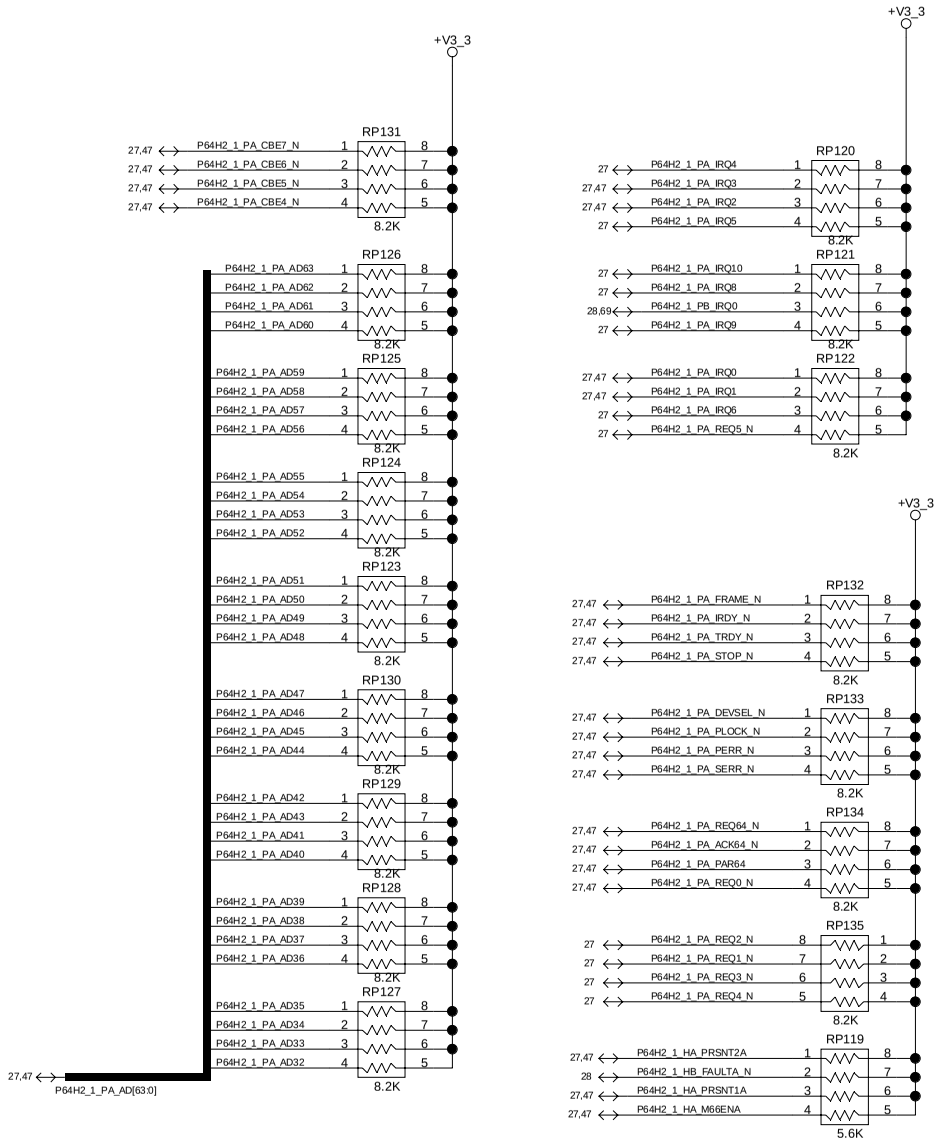




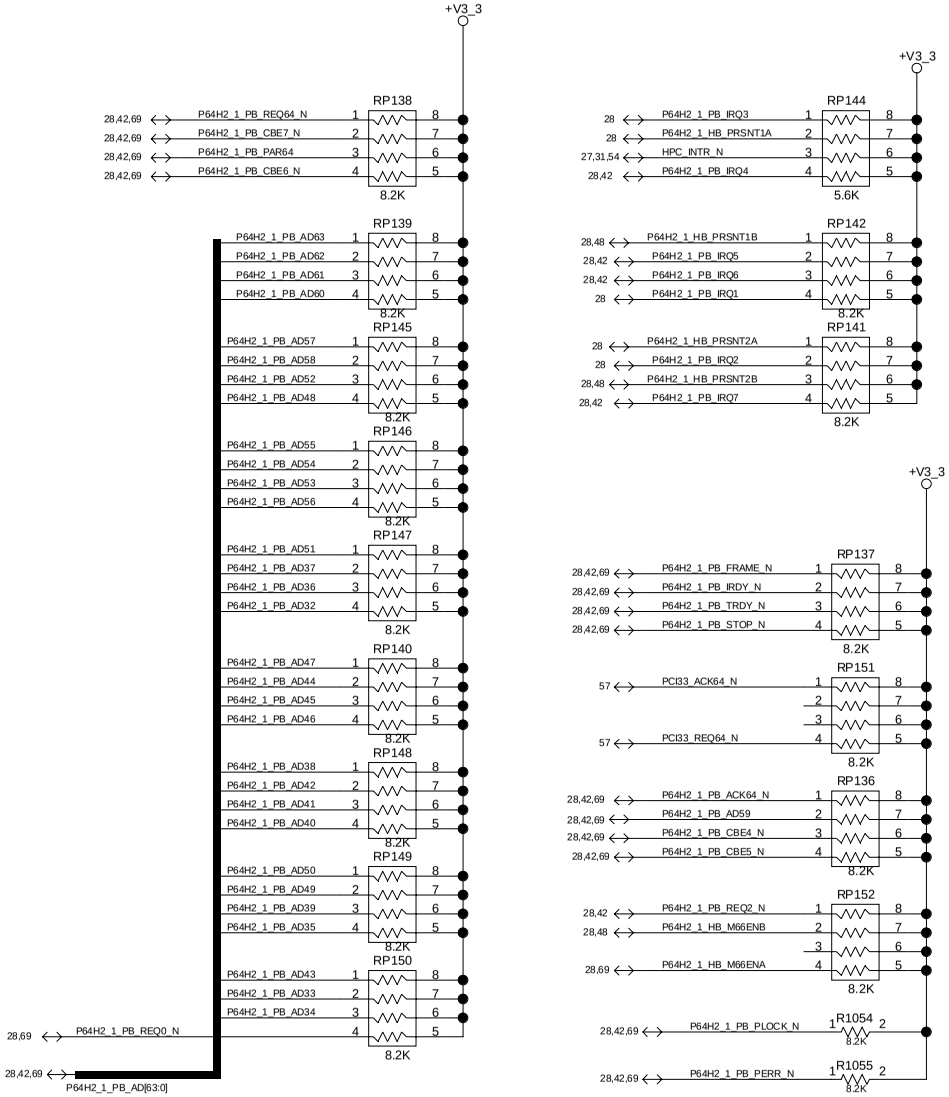


P64H2 #2 power, ground and decoupling

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	34 OF 83

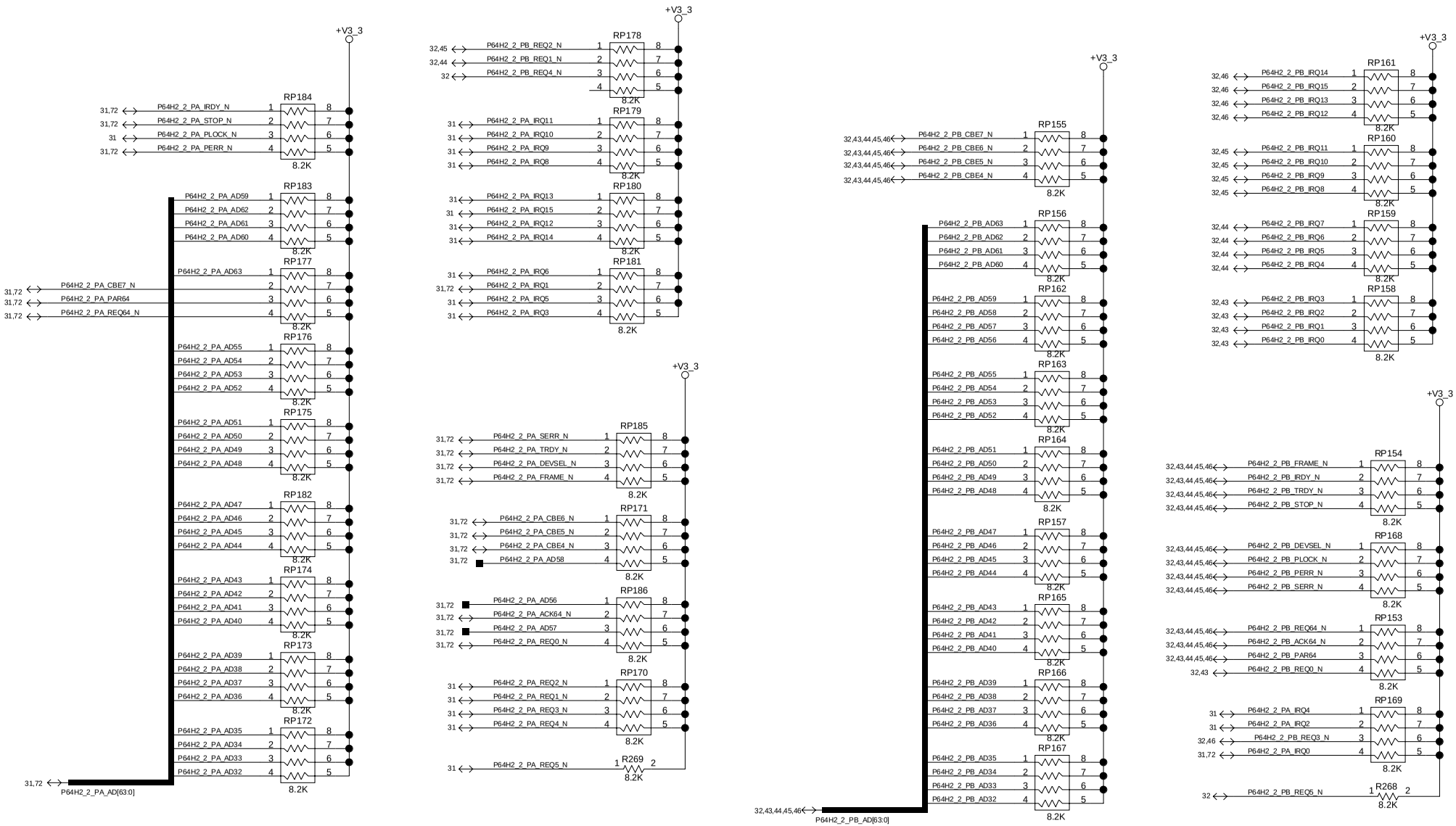


P64H2 #1 PCI Bus A pull-ups



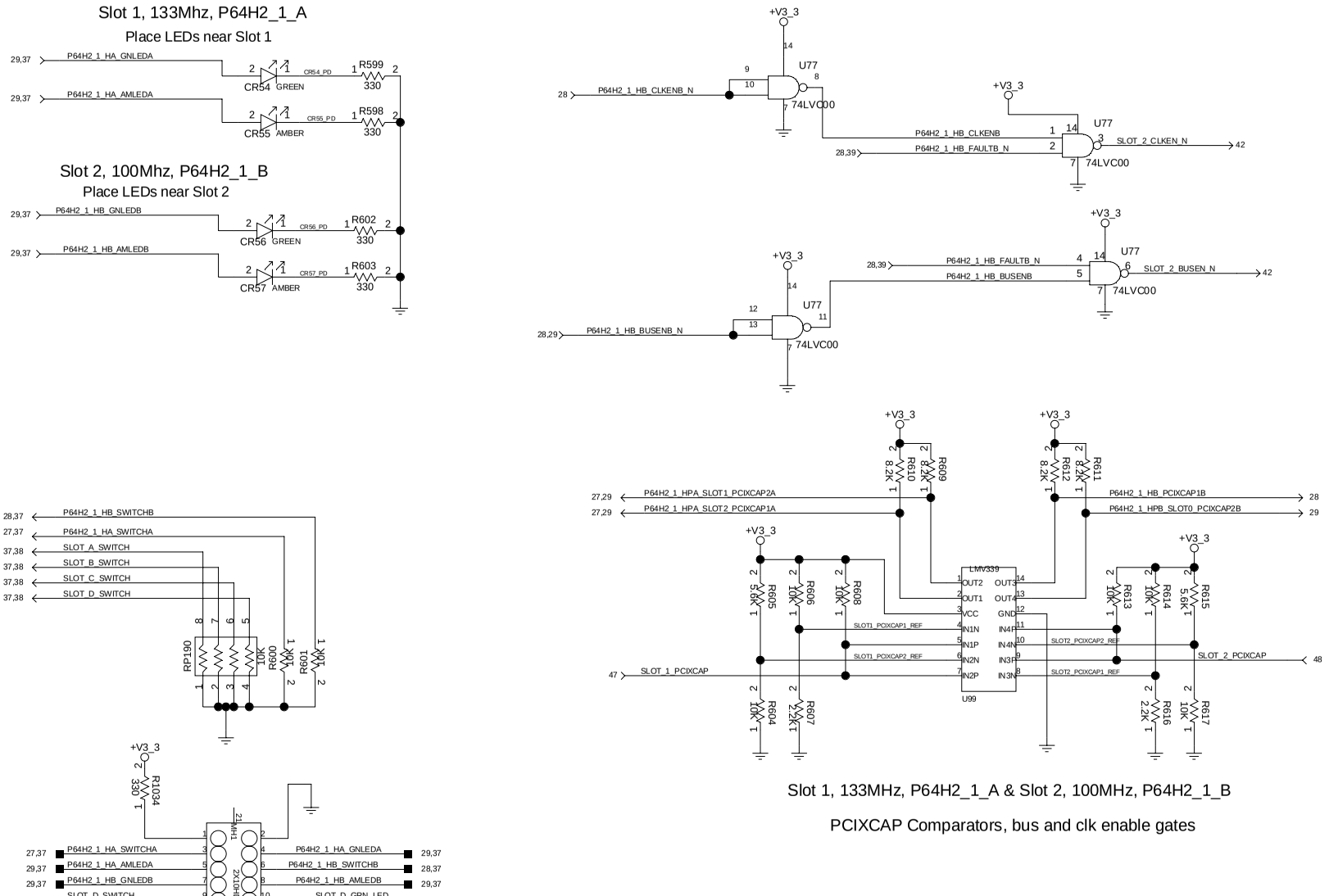
P64H2 #1 PCI Bus B pull-ups

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	35 OF 83



P64H2 #2 PCI pull-ups

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	36 OF 83



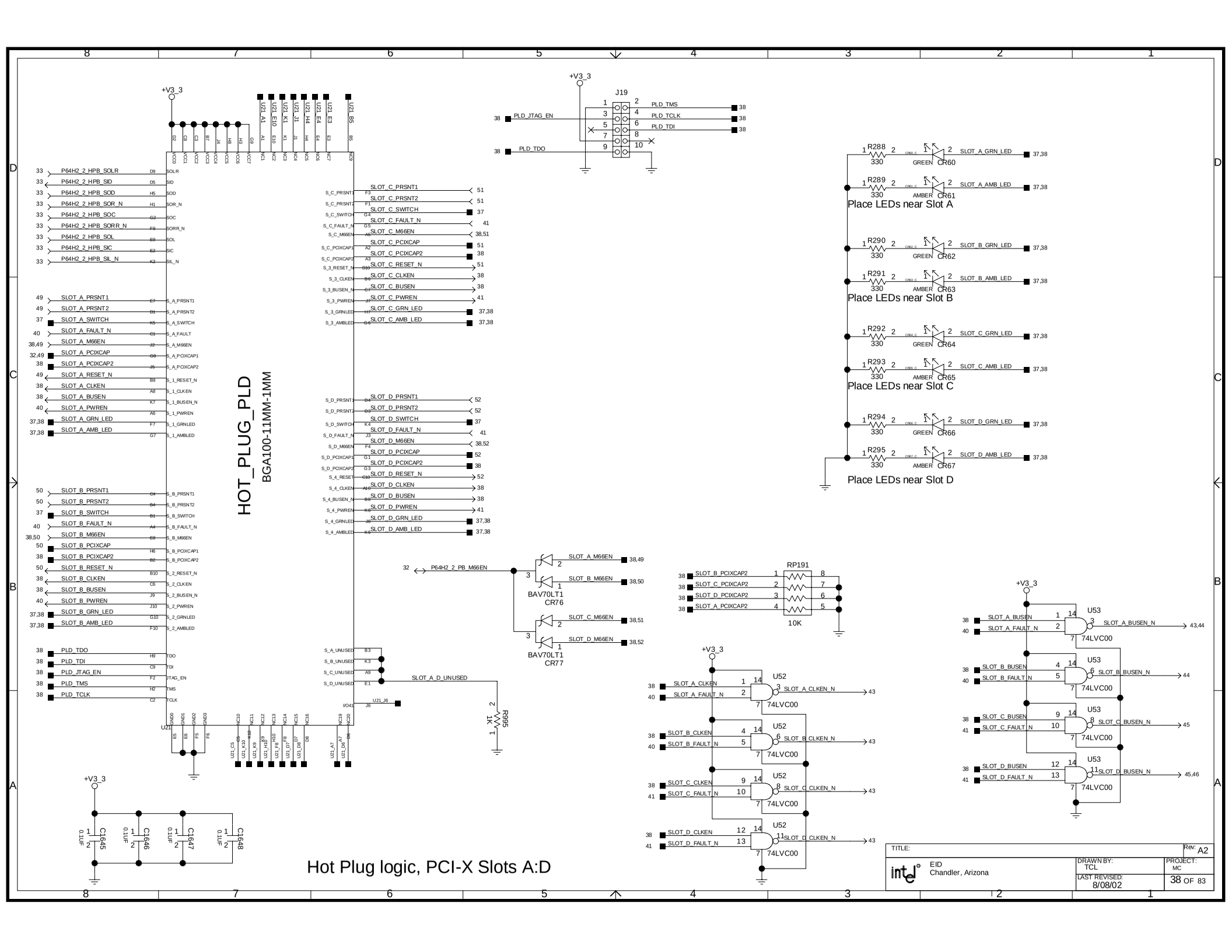
Slot 1, 133MHz, P64H2_1_A & Slot 2, 100MHz, P64H2_1_B

PCIXCAP Comparators, bus and clk enable gates

Chassis hot-plug switch board connector

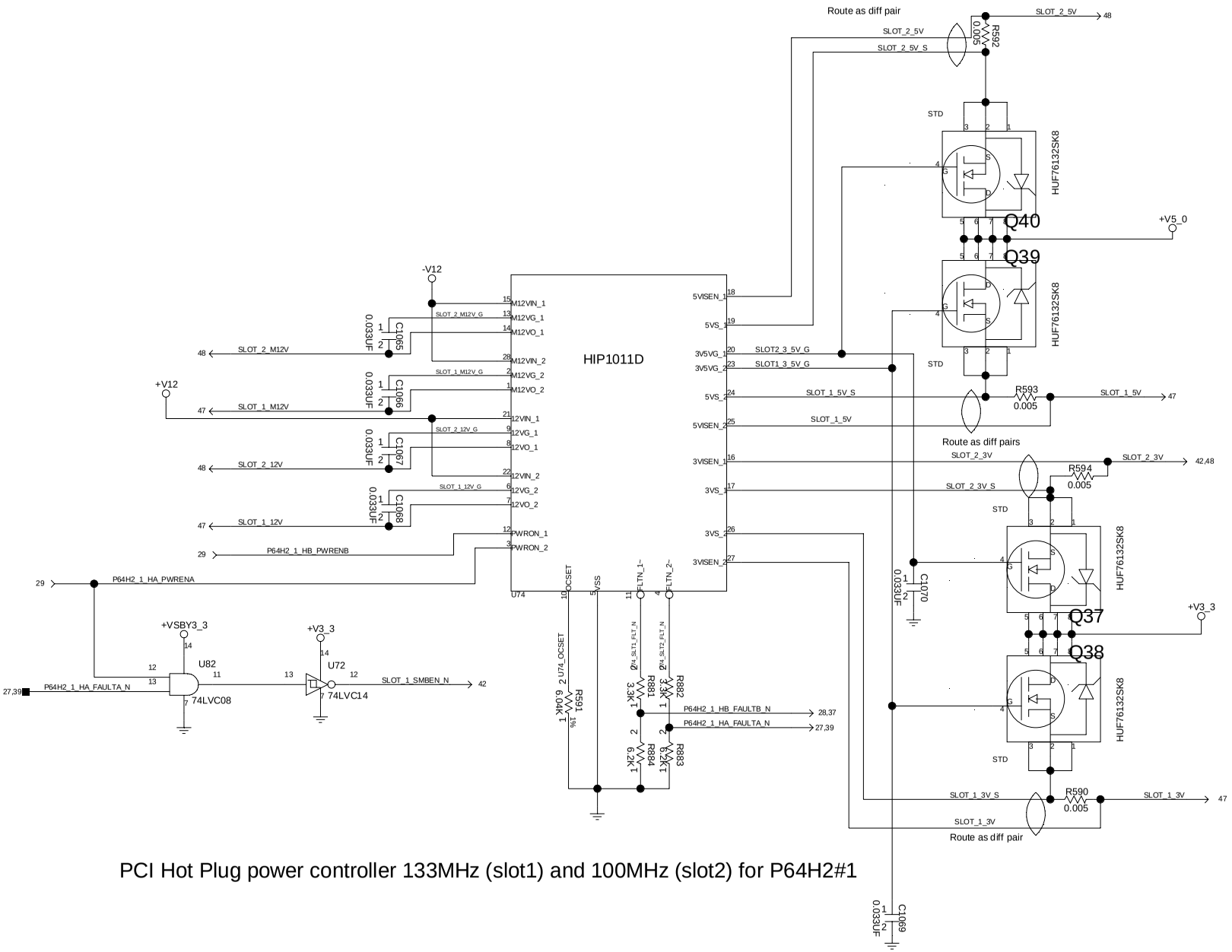
Hot Plug logic, PCI-X Slots 1,2

TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	37 OF 83	



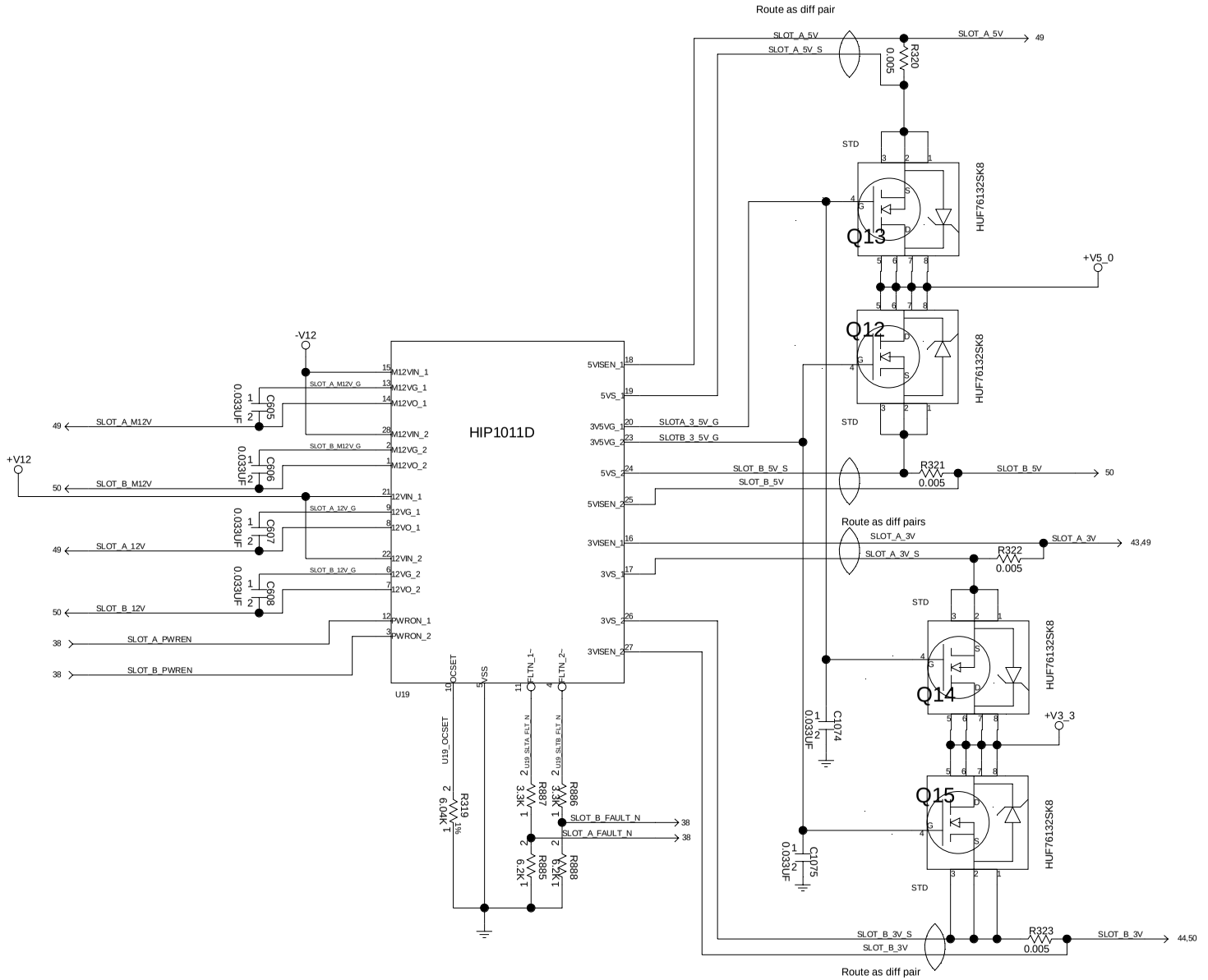
Hot Plug logic, PCI-X Slots A:D

TITLE:	Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
	LAST REVISED: 8/08/02
	38 OF 83



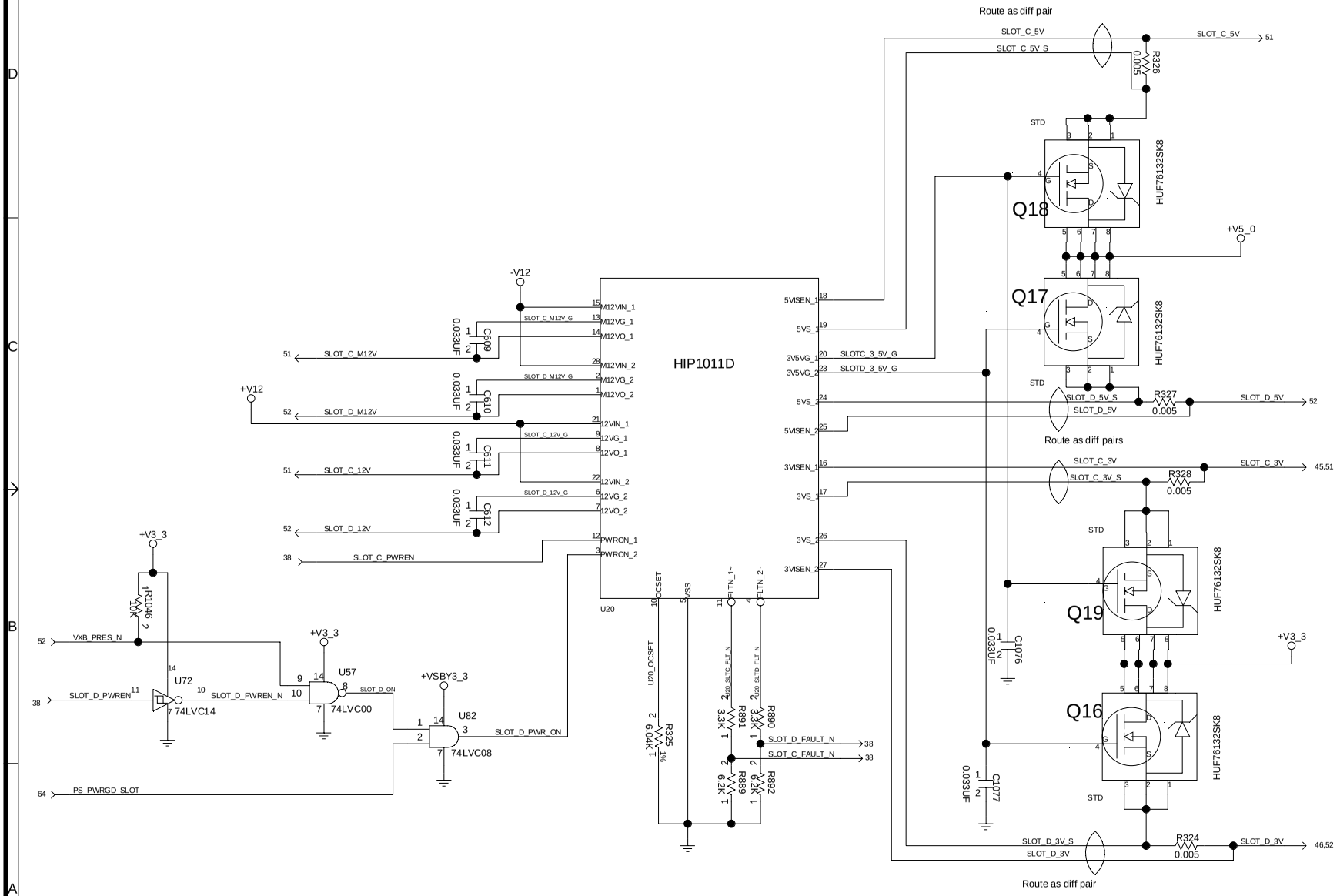
PCI Hot Plug power controller 133MHz (slot1) and 100MHz (slot2) for P64H2#1

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	39 OF 83



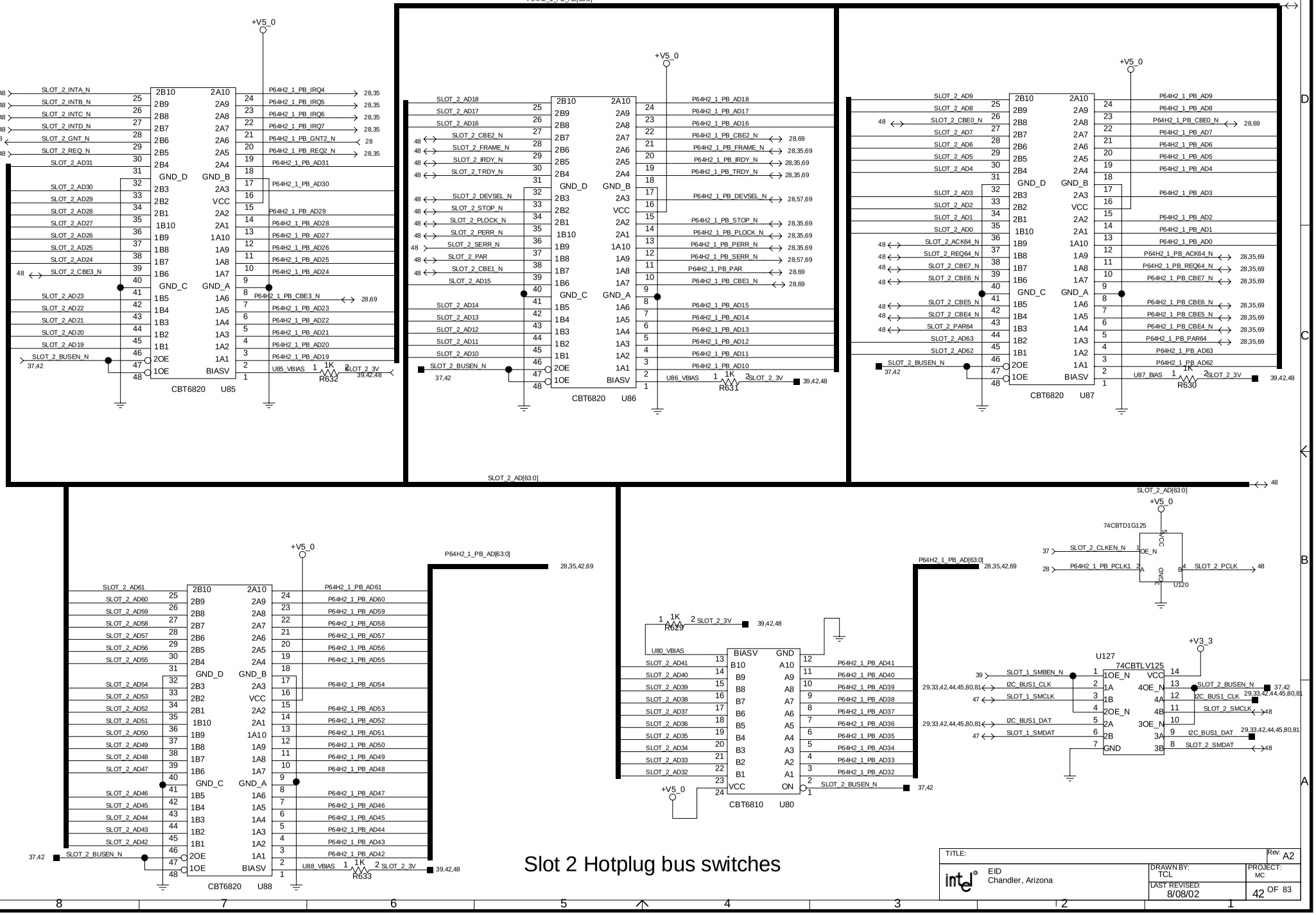
PCI Hot Plug power control. 66MHz Slots A and B

TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	40 OF 83	



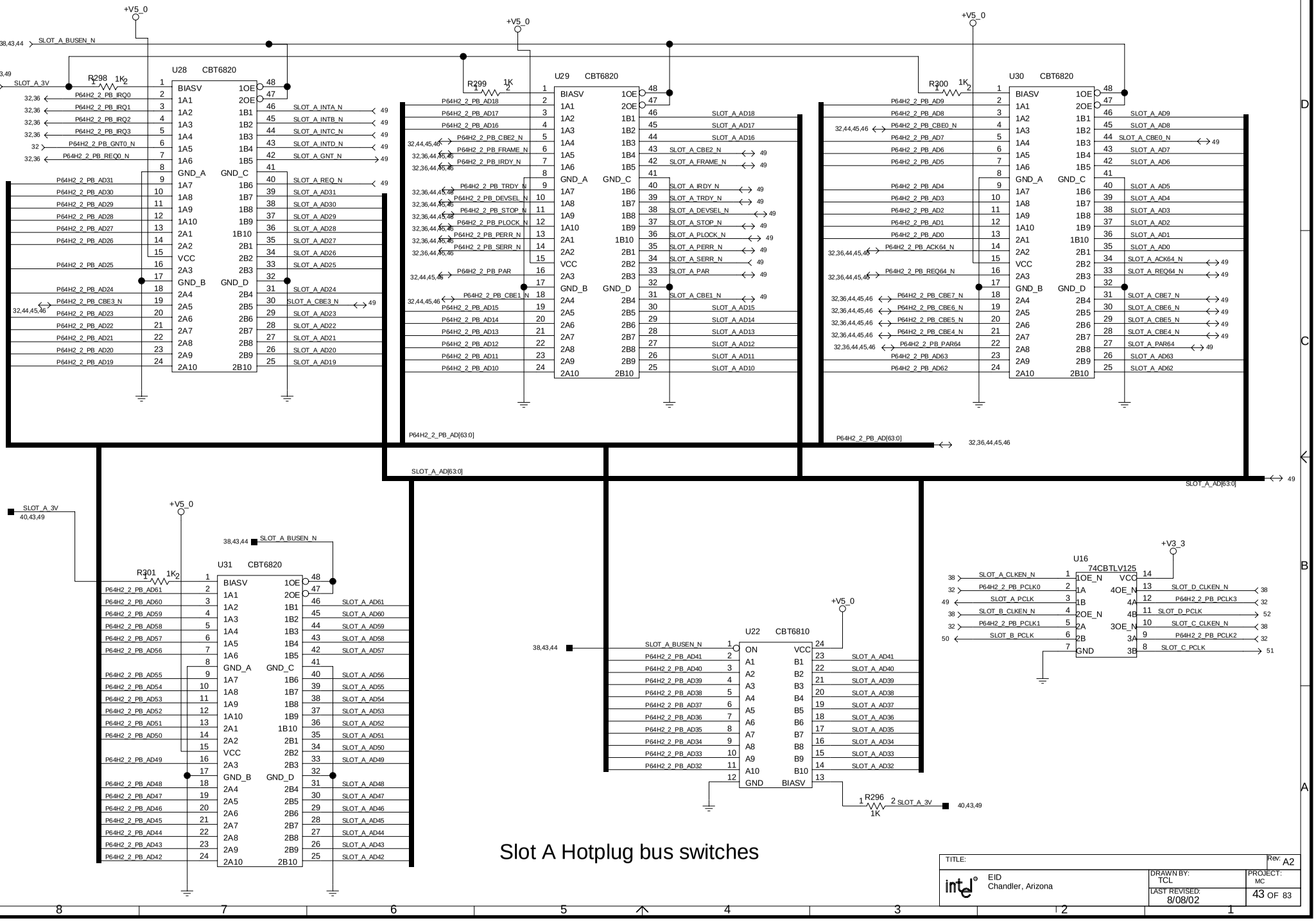
PCI Hot Plug power control. 66MHz Slots C and D

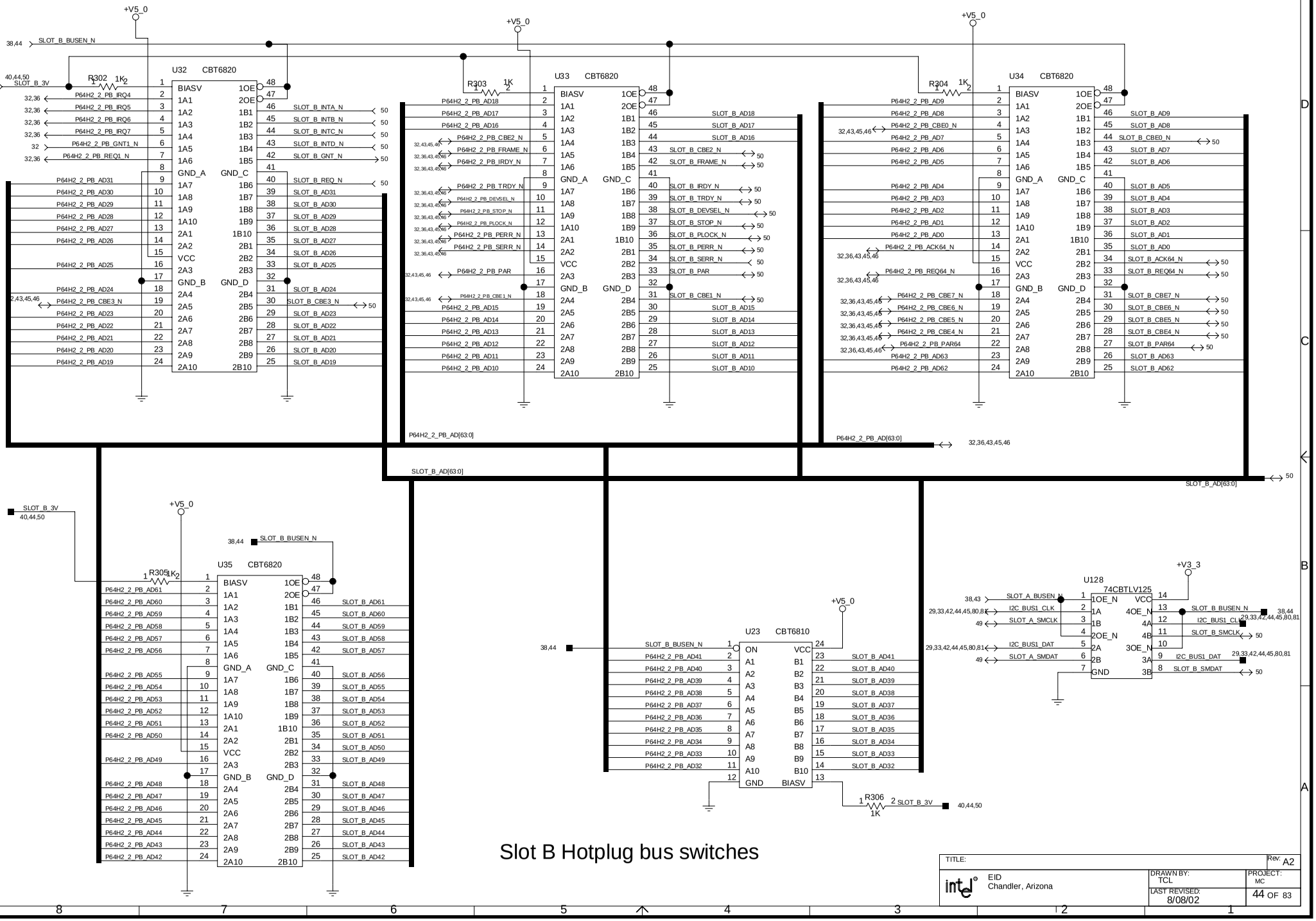
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	41 OF 83



Slot 2 Hotplug bus switches

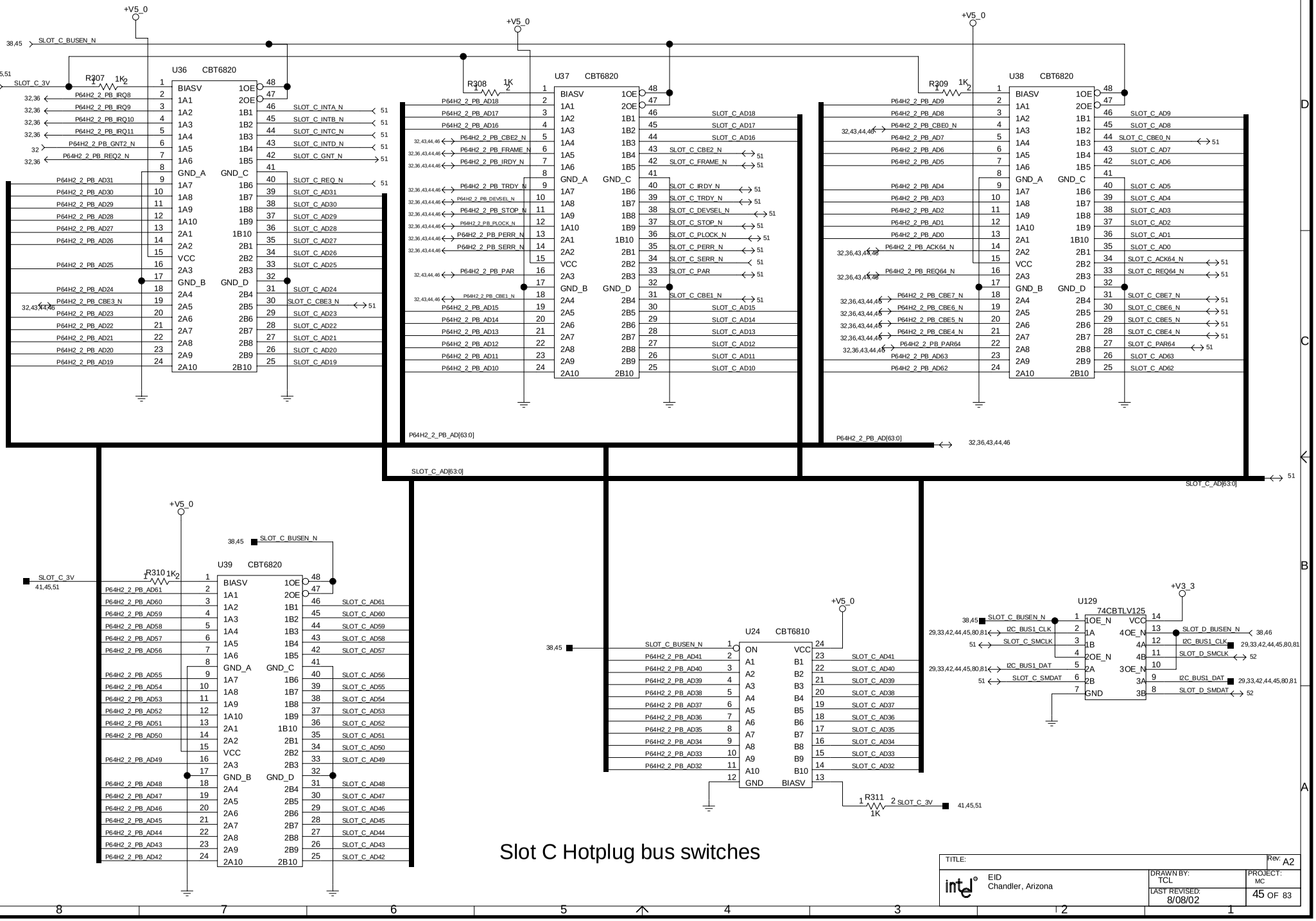
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	42 OF 83

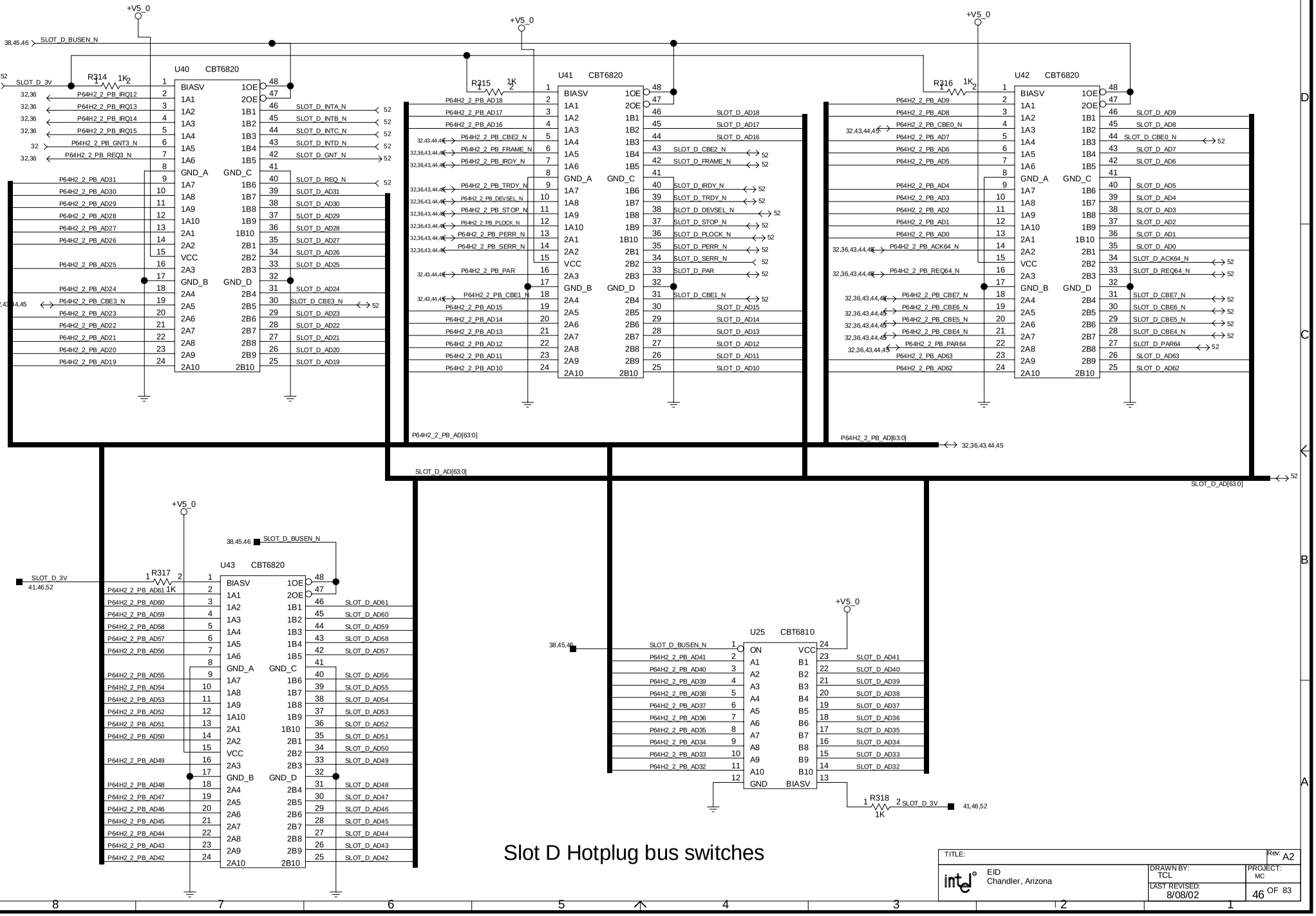

U28 CBT6820
U29 CBT6820
U30 CBT6820
U31 CBT6820
U22 CBT6810
U16 74CBTLV125
R298 1K
R299 1K
R300 1K
R301 1K
R296 1K
+V5_0
+V3_3
SLOT_A_BUSEN_N
SLOT_A_3V
P64H2_2_PB_AD[63:0]
SLOT_A_AD[63:0]
Slot A Hotplug bus switches
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
LAST REVISED: 8/08/02
PROJECT: MC
43 OF 83



Slot B Hotplug bus switches

TITLE:	Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
	LAST REVISED: 8/08/02
	44 OF 83


U36 CBT6820
U37 CBT6820
U38 CBT6820
U39 CBT6820
U24 CBT6810
U129 74CBTLV125
R307 1K
R308 1K
R309 1K
R310 1K
R311 1K
+V5_0
+V3_3
SLOT_C_BUSEN_N
SLOT_C_3V
P64H2_2_PB_AD[63:0]
SLOT_C_AD[63:0]
Slot C Hotplug bus switches
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
LAST REVISED: 8/08/02
PROJECT: MC
45 OF 83


+V5_0
38,45,46 SLOT_D_BUSEN_N
41,46,52 SLOT_D_3V
R314 1K
U40 CBT6820
BIASV 1OE
1A1 2OE
1A2 1B1
1A3 1B2
1A4 1B3
1A5 1B4
1A6 1B5
GND_A GND_C
1A7 1B6
1A8 1B7
1A9 1B8
1A10 1B9
2A1 1B10
2A2 2B1
VCC 2B2
2A3 2B3
GND_B GND_D
2A4 2B4
2A5 2B5
2A6 2B6
2A7 2B7
2A8 2B8
2A9 2B9
2A10 2B10
32,36 P64H2_2_PB_IRQ12
32,36 P64H2_2_PB_IRQ13
32,36 P64H2_2_PB_IRQ14
32,36 P64H2_2_PB_IRQ15
32 P64H2_2_PB_GNT3_N
32,36 P64H2_2_PB_REQ3_N
SLOT_D_INTA_N
SLOT_D_INTB_N
SLOT_D_INTC_N
SLOT_D_INTD_N
SLOT_D_GNT_N
SLOT_D_REQ_N
SLOT_D_AD31
SLOT_D_AD30
SLOT_D_AD29
SLOT_D_AD28
SLOT_D_AD27
SLOT_D_AD26
SLOT_D_AD25
SLOT_D_AD24
SLOT_D_CBE3_N
SLOT_D_AD23
SLOT_D_AD22
SLOT_D_AD21
SLOT_D_AD20
SLOT_D_AD19
P64H2_2_PB_AD31
P64H2_2_PB_AD30
P64H2_2_PB_AD29
P64H2_2_PB_AD28
P64H2_2_PB_AD27
P64H2_2_PB_AD26
P64H2_2_PB_AD25
P64H2_2_PB_AD24
32,43,44,45 P64H2_2_PB_CBE3_N
P64H2_2_PB_AD23
P64H2_2_PB_AD22
P64H2_2_PB_AD21
P64H2_2_PB_AD20
P64H2_2_PB_AD19
R315 1K
U41 CBT6820
P64H2_2_PB_AD18
P64H2_2_PB_AD17
P64H2_2_PB_AD16
32,43,44,45 P64H2_2_PB_CBE2_N
32,36,43,44,45 P64H2_2_PB_FRAME_N
32,36,43,44,45 P64H2_2_PB_IRDY_N
32,36,43,44,45 P64H2_2_PB_TRDY_N
32,36,43,44,45 P64H2_2_PB_DEVSEL_N
32,36,43,44,45 P64H2_2_PB_STOP_N
32,36,43,44,45 P64H2_2_PB_PLOCK_N
32,36,43,44,45 P64H2_2_PB_PERR_N
32,36,43,44,45 P64H2_2_PB_SERR_N
32,43,44,45 P64H2_2_PB_PAR
32,43,44,45 P64H2_2_PB_CBE1_N
P64H2_2_PB_AD15
P64H2_2_PB_AD14
P64H2_2_PB_AD13
P64H2_2_PB_AD12
P64H2_2_PB_AD11
P64H2_2_PB_AD10
SLOT_D_AD18
SLOT_D_AD17
SLOT_D_AD16
SLOT_D_CBE2_N
SLOT_D_FRAME_N
SLOT_D_IRDY_N
SLOT_D_TRDY_N
SLOT_D_DEVSEL_N
SLOT_D_STOP_N
SLOT_D_PLOCK_N
SLOT_D_PERR_N
SLOT_D_SERR_N
SLOT_D_PAR
SLOT_D_CBE1_N
SLOT_D_AD15
SLOT_D_AD14
SLOT_D_AD13
SLOT_D_AD12
SLOT_D_AD11
SLOT_D_AD10
P64H2_2_PB_AD[63:0]
R316 1K
U42 CBT6820
P64H2_2_PB_AD9
P64H2_2_PB_AD8
32,43,44,45 P64H2_2_PB_CBE0_N
P64H2_2_PB_AD7
P64H2_2_PB_AD6
P64H2_2_PB_AD5
P64H2_2_PB_AD4
P64H2_2_PB_AD3
P64H2_2_PB_AD2
P64H2_2_PB_AD1
P64H2_2_PB_AD0
32,36,43,44,45 P64H2_2_PB_ACK64_N
32,36,43,44,45 P64H2_2_PB_REQ64_N
32,36,43,44,45 P64H2_2_PB_CBE7_N
32,36,43,44,45 P64H2_2_PB_CBE6_N
32,36,43,44,45 P64H2_2_PB_CBE5_N
32,36,43,44,45 P64H2_2_PB_CBE4_N
32,36,43,44,45 P64H2_2_PB_PAR64
P64H2_2_PB_AD63
P64H2_2_PB_AD62
SLOT_D_AD9
SLOT_D_AD8
SLOT_D_CBE0_N
SLOT_D_AD7
SLOT_D_AD6
SLOT_D_AD5
SLOT_D_AD4
SLOT_D_AD3
SLOT_D_AD2
SLOT_D_AD1
SLOT_D_AD0
SLOT_D_ACK64_N
SLOT_D_REQ64_N
SLOT_D_CBE7_N
SLOT_D_CBE6_N
SLOT_D_CBE5_N
SLOT_D_CBE4_N
SLOT_D_PAR64
SLOT_D_AD63
SLOT_D_AD62
P64H2_2_PB_AD[63:0]
32,36,43,44,45
SLOT_D_AD[63:0]
52
R317 1K
U43 CBT6820
P64H2_2_PB_AD61
P64H2_2_PB_AD60
P64H2_2_PB_AD59
P64H2_2_PB_AD58
P64H2_2_PB_AD57
P64H2_2_PB_AD56
P64H2_2_PB_AD55
P64H2_2_PB_AD54
P64H2_2_PB_AD53
P64H2_2_PB_AD52
P64H2_2_PB_AD51
P64H2_2_PB_AD50
P64H2_2_PB_AD49
P64H2_2_PB_AD48
P64H2_2_PB_AD47
P64H2_2_PB_AD46
P64H2_2_PB_AD45
P64H2_2_PB_AD44
P64H2_2_PB_AD43
P64H2_2_PB_AD42
SLOT_D_AD61
SLOT_D_AD60
SLOT_D_AD59
SLOT_D_AD58
SLOT_D_AD57
SLOT_D_AD56
SLOT_D_AD55
SLOT_D_AD54
SLOT_D_AD53
SLOT_D_AD52
SLOT_D_AD51
SLOT_D_AD50
SLOT_D_AD49
SLOT_D_AD48
SLOT_D_AD47
SLOT_D_AD46
SLOT_D_AD45
SLOT_D_AD44
SLOT_D_AD43
SLOT_D_AD42
U25 CBT6810
ON VCC
A1 B1
A2 B2
A3 B3
A4 B4
A5 B5
A6 B6
A7 B7
A8 B8
A9 B9
A10 B10
GND BIASV
P64H2_2_PB_AD41
P64H2_2_PB_AD40
P64H2_2_PB_AD39
P64H2_2_PB_AD38
P64H2_2_PB_AD37
P64H2_2_PB_AD36
P64H2_2_PB_AD35
P64H2_2_PB_AD34
P64H2_2_PB_AD33
P64H2_2_PB_AD32
SLOT_D_AD41
SLOT_D_AD40
SLOT_D_AD39
SLOT_D_AD38
SLOT_D_AD37
SLOT_D_AD36
SLOT_D_AD35
SLOT_D_AD34
SLOT_D_AD33
SLOT_D_AD32
R318 1K
SLOT_D_3V
41,46,52
Slot D Hotplug bus switches
TITLE:
Rev: A2
intel
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
LAST REVISED: 8/08/02
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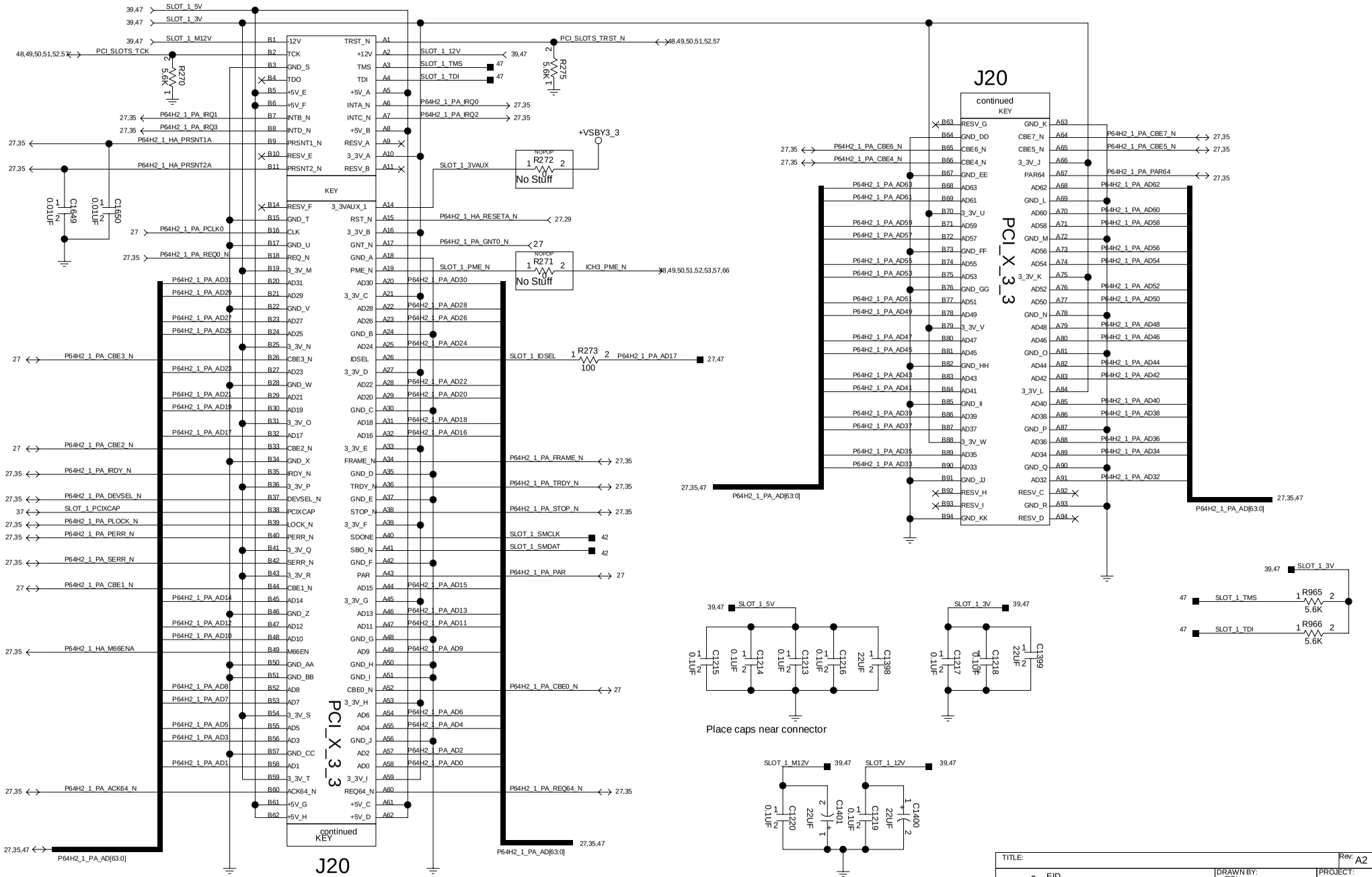
PCI-X Slot 1 (P64H2 #1, PCI Bus A)



TITLE:	Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
	LAST REVISED: 8/08/02
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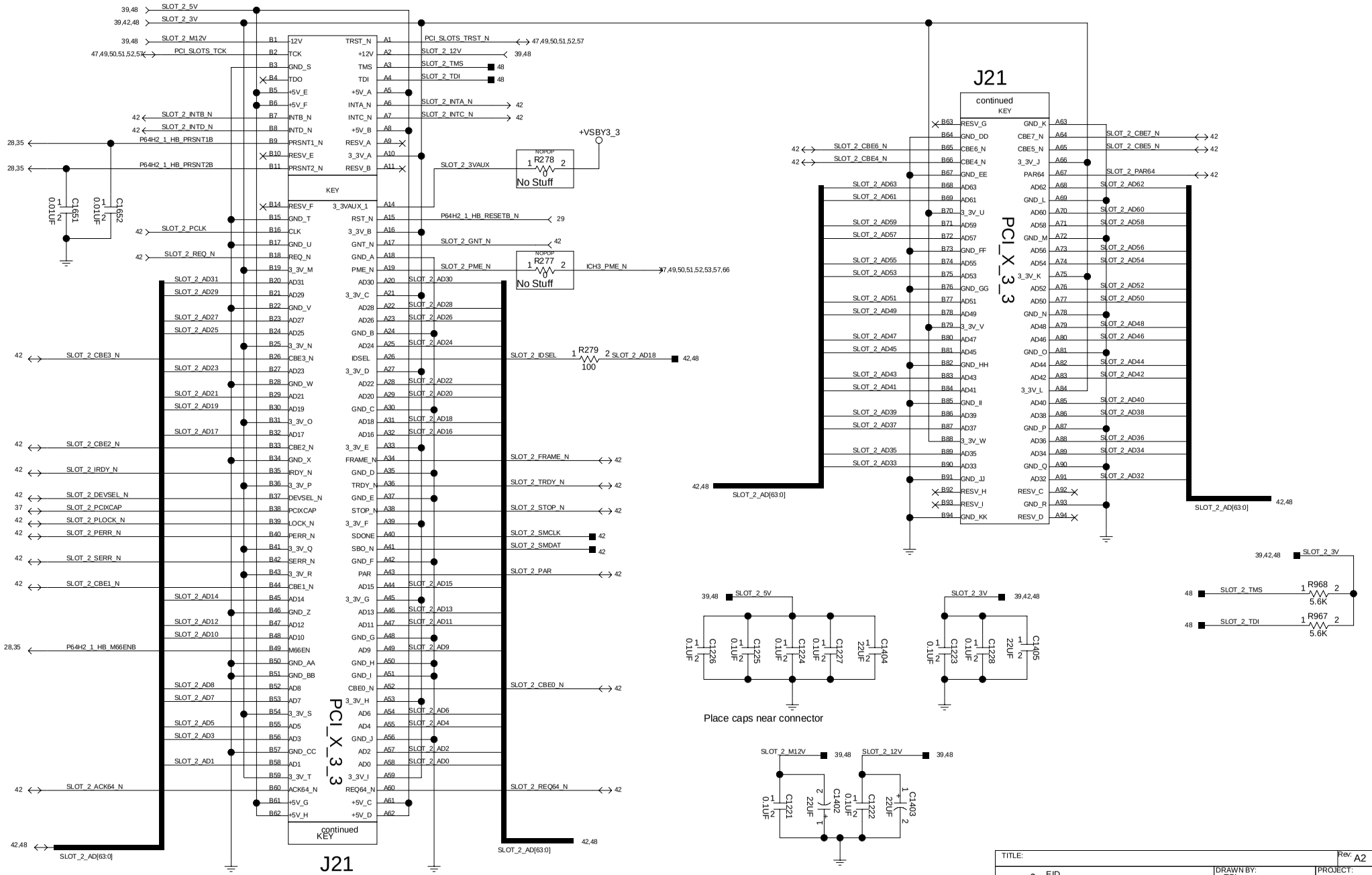
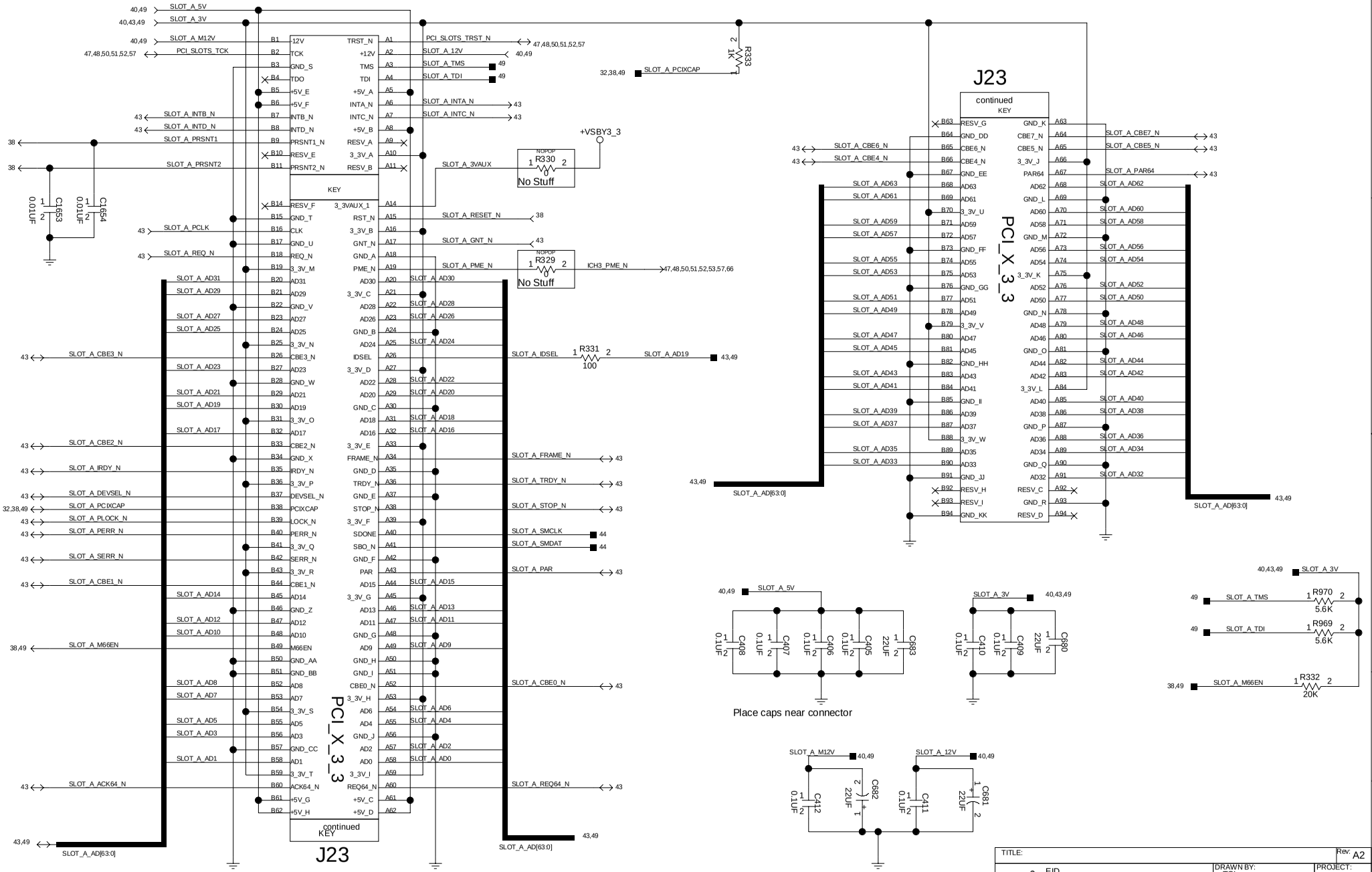
PCI-X Slot 2 (P64H2 #1, PCI Bus B)



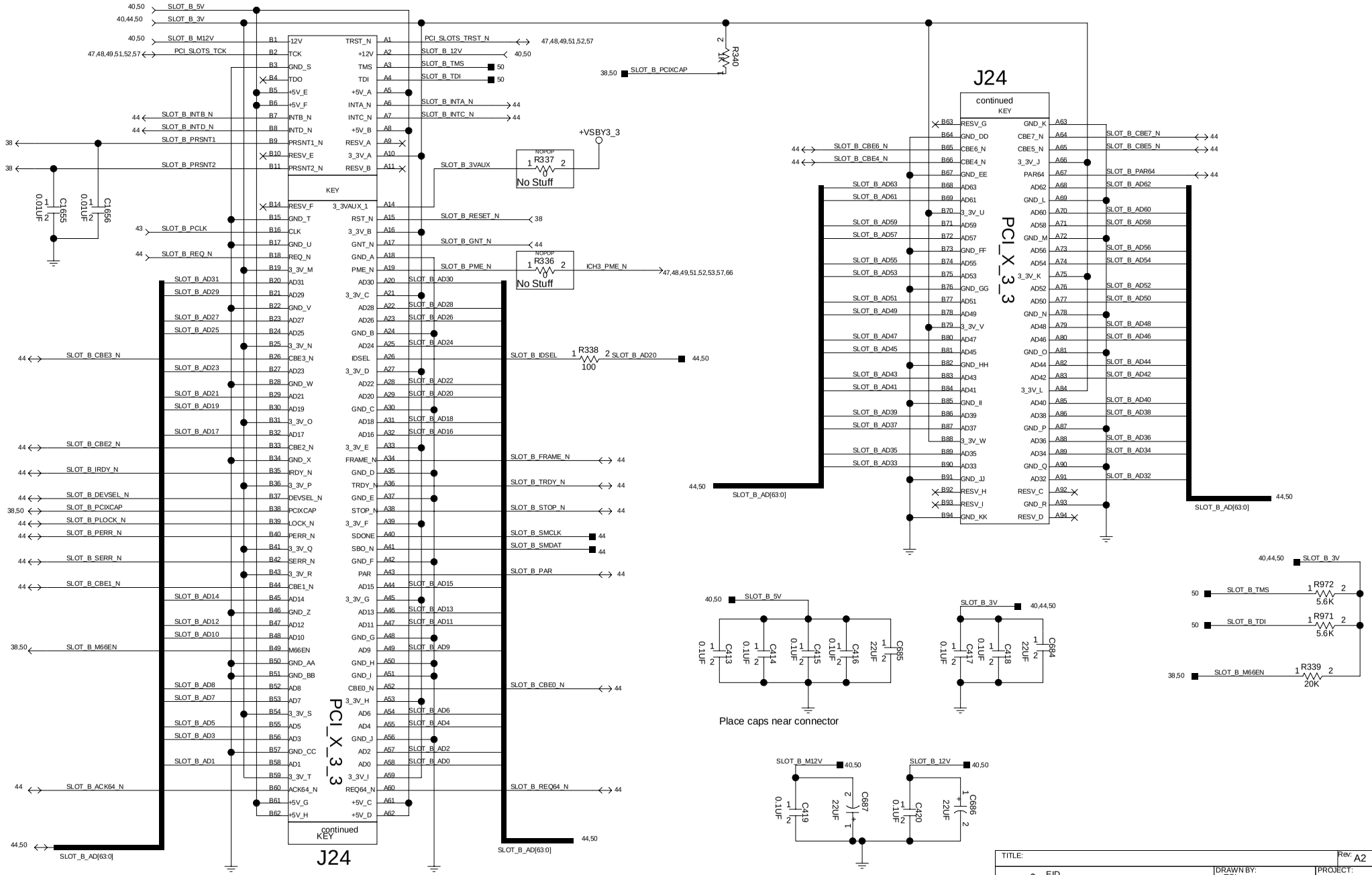
TITLE:	Rev: A2
EID Chandler, Arizona	DRAWN BY: TCL PROJECT: MC LAST REVISED: 8/08/02 48 OF 83

PCI-X 66MHz SLOT A



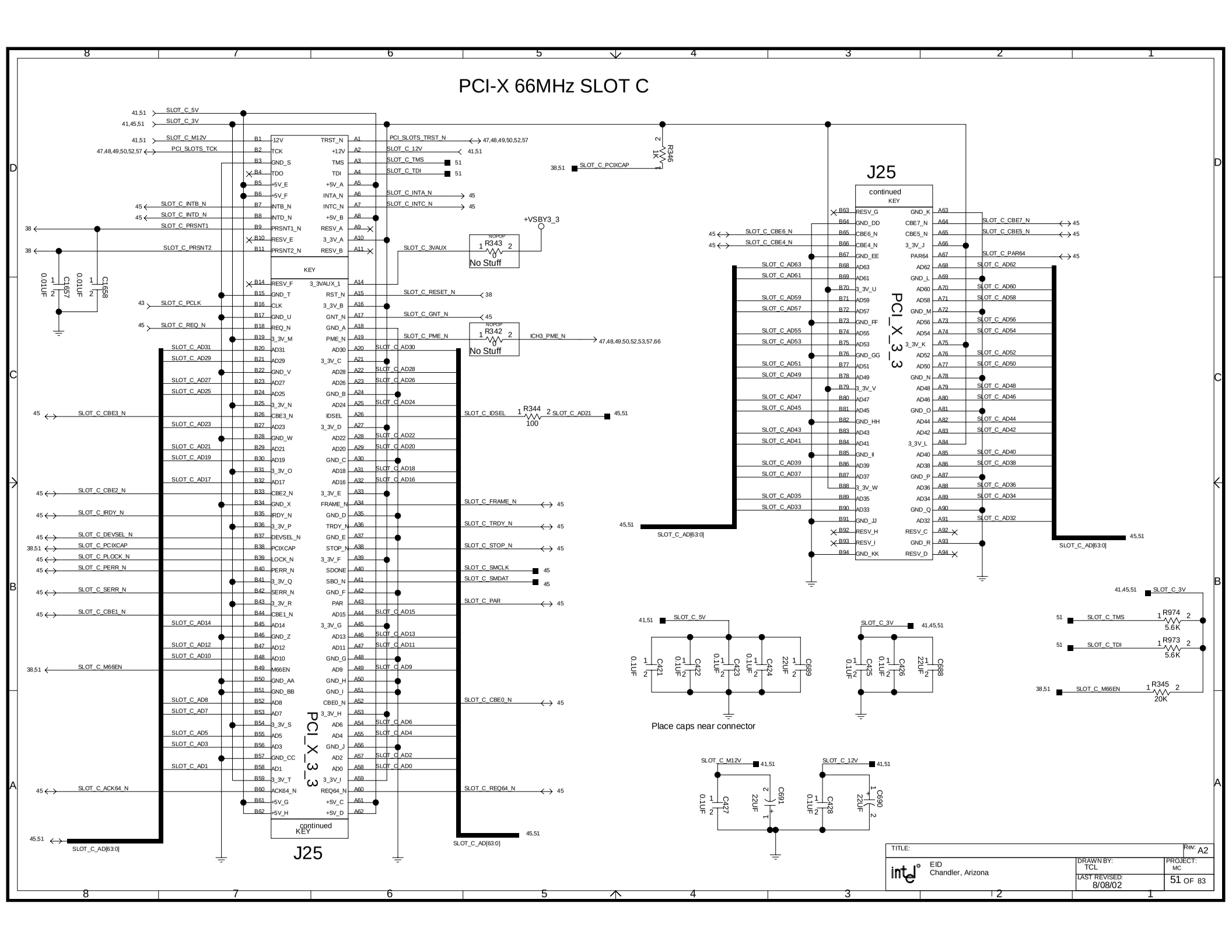
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	49 OF 83

PCI-X 66MHz SLOT B



TITLE:	Rev: A2
EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
	LAST REVISED: 8/08/02
	50 OF 83

PCI-X 66MHz SLOT C



TITLE:

Rev: A2

intel EID Chandler, Arizona

DRAWN BY: TCL

PROJECT: MC

LAST REVISED: 8/08/02

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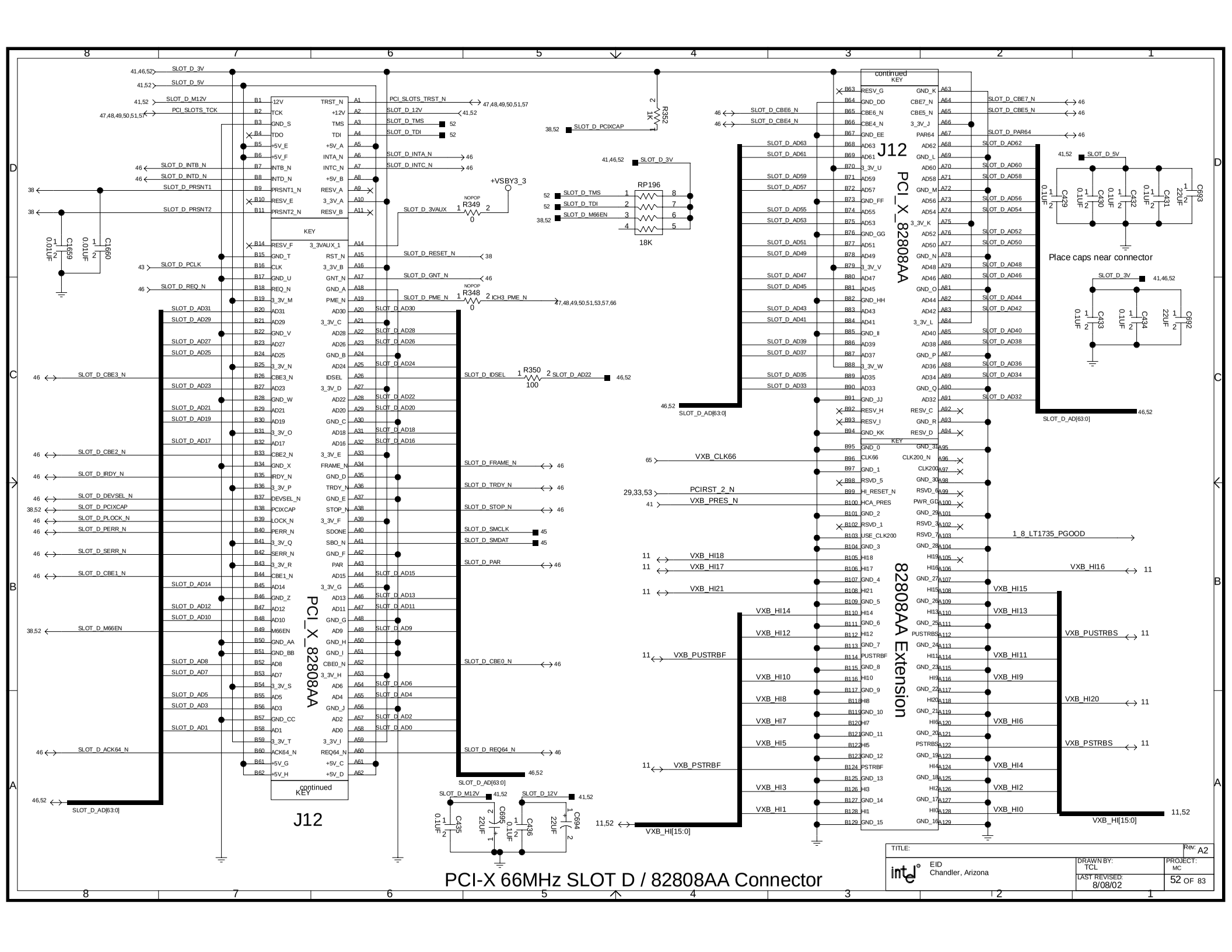
PCI-X 66MHz SLOT D / 82808AA Connector
PCI_X_82808AA
82808AA Extension
J12
KEY
continued
Place caps near connector
SLOT_D_AD[63:0]
VXB_HI[15:0]
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
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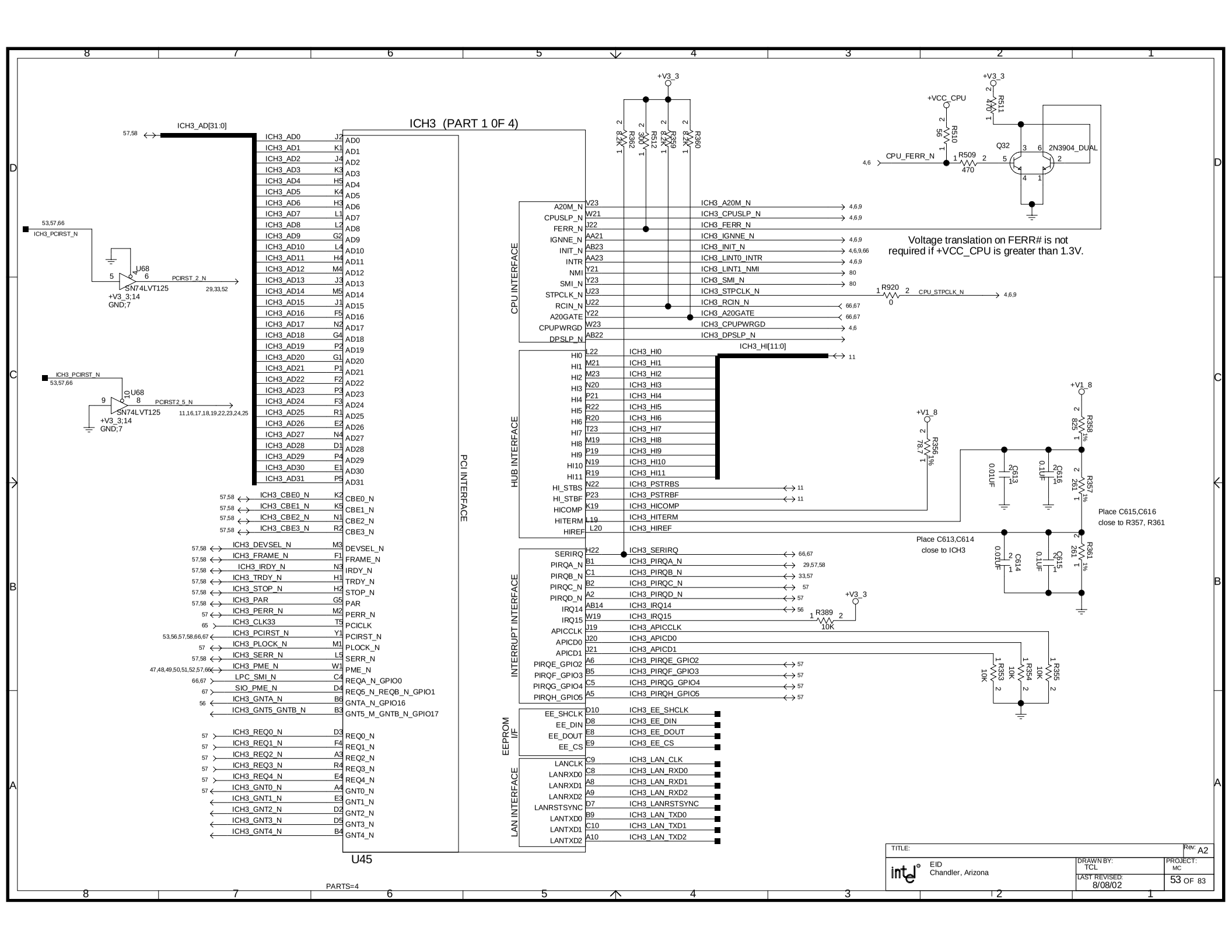
ICH3 (PART 1 0F 4)
U45
PCI INTERFACE
CPU INTERFACE
HUB INTERFACE
INTERRUPT INTERFACE
EEPROM I/F
LAN INTERFACE
ICH3_AD[31:0]
ICH3_HI[11:0]
Voltage translation on FERR# is not required if +VCC_CPU is greater than 1.3V.
Place C615,C616 close to R357, R361
Place C613,C614 close to ICH3
SN74LVT125
2N3904_DUAL
PARTS=4
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
LAST REVISED: 8/08/02
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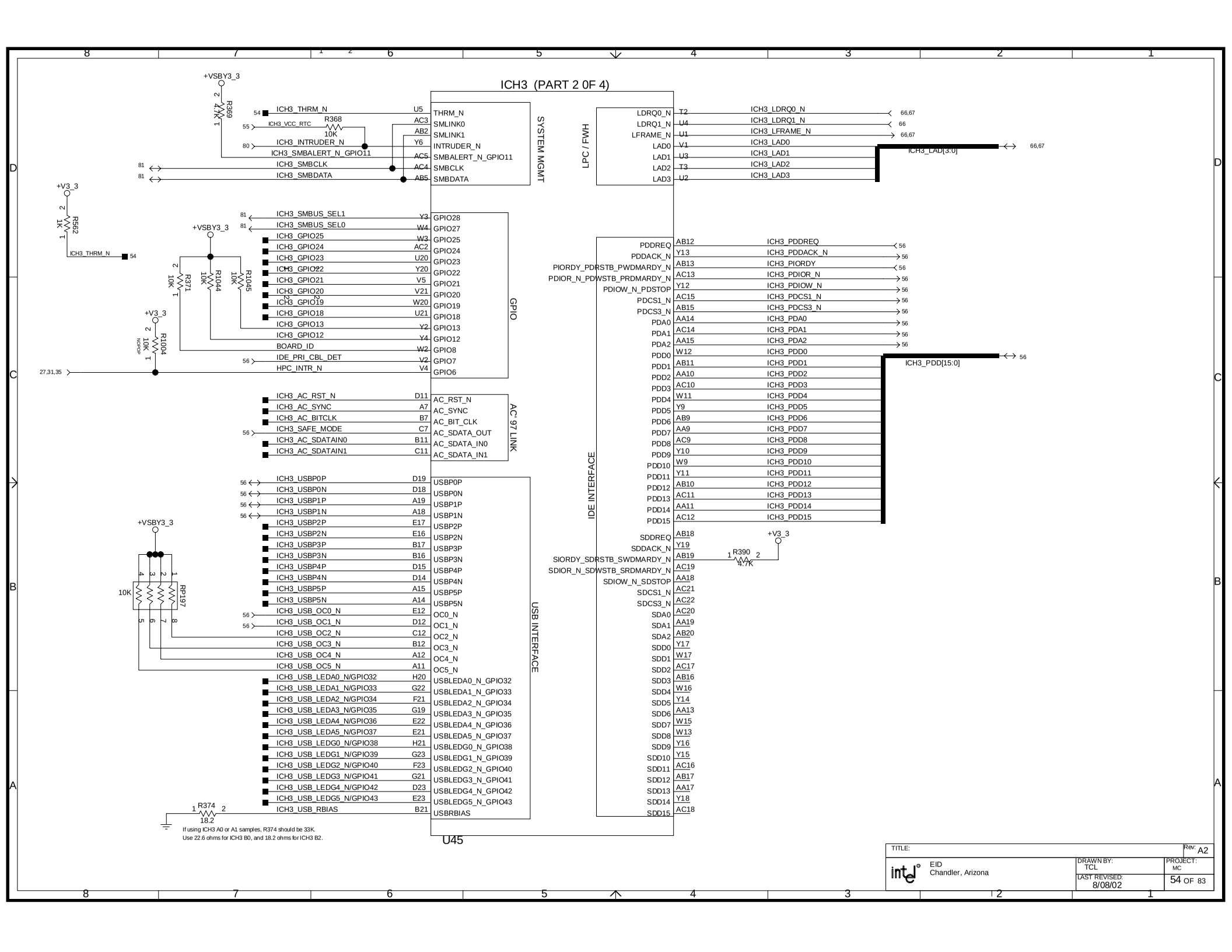
ICH3 (PART 2 0F 4)
SYSTEM MGMT
GPIO
AC' 97 LINK
USB INTERFACE
LPC / FWH
IDE INTERFACE
U45
THRM_N
SMLINK0
SMLINK1
INTRUDER_N
SMBALERT_N_GPIO11
SMBCLK
SMBDATA
GPIO28
GPIO27
GPIO25
GPIO24
GPIO23
GPIO22
GPIO21
GPIO20
GPIO19
GPIO18
GPIO13
GPIO12
GPIO8
GPIO7
GPIO6
AC_RST_N
AC_SYNC
AC_BIT_CLK
AC_SDATA_OUT
AC_SDATA_IN0
AC_SDATA_IN1
USBP0P
USBP0N
USBP1P
USBP1N
USBP2P
USBP2N
USBP3P
USBP3N
USBP4P
USBP4N
USBP5P
USBP5N
OC0_N
OC1_N
OC2_N
OC3_N
OC4_N
OC5_N
USBLEDA0_N_GPIO32
USBLEDA1_N_GPIO33
USBLEDA2_N_GPIO34
USBLEDA3_N_GPIO35
USBLEDA4_N_GPIO36
USBLEDA5_N_GPIO37
USBLEDG0_N_GPIO38
USBLEDG1_N_GPIO39
USBLEDG2_N_GPIO40
USBLEDG3_N_GPIO41
USBLEDG4_N_GPIO42
USBLEDG5_N_GPIO43
USBRBIAS
LDRQ0_N
LDRQ1_N
LFRAME_N
LAD0
LAD1
LAD2
LAD3
PDDREQ
PDDACK_N
PIORDY_PDRSTB_PWDMARDY_N
PDIOR_N_PDWSTB_PRDMARDY_N
PDIOW_N_PDSTOP
PDCS1_N
PDCS3_N
PDA0
PDA1
PDA2
PDD0
PDD1
PDD2
PDD3
PDD4
PDD5
PDD6
PDD7
PDD8
PDD9
PDD10
PDD11
PDD12
PDD13
PDD14
PDD15
SDDREQ
SDDACK_N
SIORDY_SDRSTB_SWDMARDY_N
SDIOR_N_SDWSTB_SRDMARDY_N
SDIOW_N_SDSTOP
SDCS1_N
SDCS3_N
SDA0
SDA1
SDA2
SDD0
SDD1
SDD2
SDD3
SDD4
SDD5
SDD6
SDD7
SDD8
SDD9
SDD10
SDD11
SDD12
SDD13
SDD14
SDD15
ICH3_LAD[3:0]
ICH3_PDD[15:0]
+VSBY3_3
+V3_3
R369 8.2K
R368 10K
R562 1K
R371 10K
R1044 10K
R1045 10K
R1004 10K NOPOP
RP197 10K
R390 4.7K
R374 18.2
If using ICH3 A0 or A1 samples, R374 should be 33K.
Use 22.6 ohms for ICH3 B0, and 18.2 ohms for ICH3 B2.
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
LAST REVISED: 8/08/02
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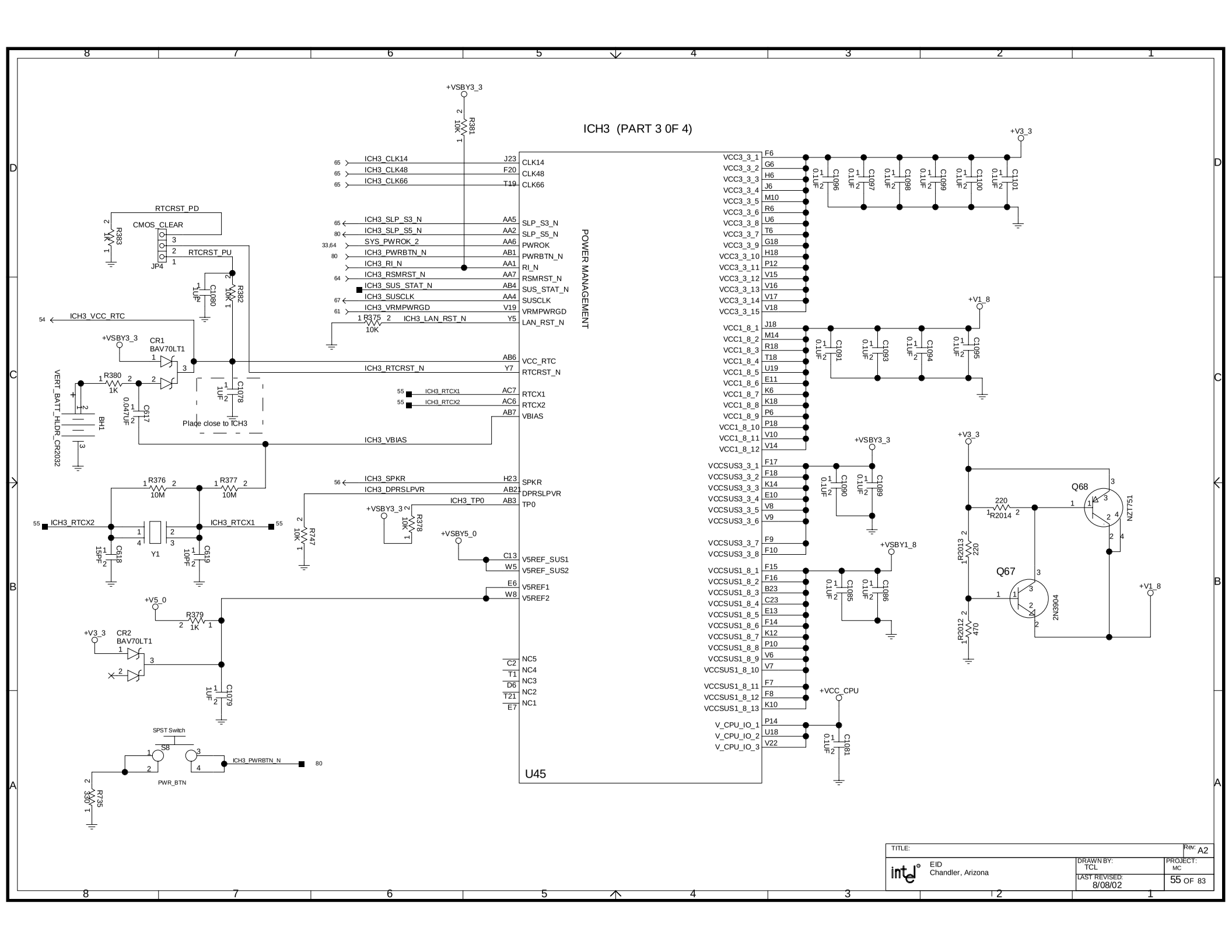
ICH3 (PART 3 0F 4)
U45
POWER MANAGEMENT
+VSBY3_3
+V3_3
+V1_8
+VSBY5_0
+VSBY1_8
+VCC_CPU
+V5_0
RTCRST_PD
CMOS_CLEAR
RTCRST_PU
JP4
ICH3_VCC_RTC
CR1
BAV70LT1
CR2
VERT_BATT_HLDR_CR2032
BH1
Place close to ICH3
ICH3_VBIAS
ICH3_RTCX1
ICH3_RTCX2
Y1
ICH3_SPKR
ICH3_DPRSLPVR
ICH3_TP0
ICH3_CLK14
ICH3_CLK48
ICH3_CLK66
ICH3_SLP_S3_N
ICH3_SLP_S5_N
SYS_PWROK_2
ICH3_PWRBTN_N
ICH3_RI_N
ICH3_RSMRST_N
ICH3_SUS_STAT_N
ICH3_SUSCLK
ICH3_VRMPWRGD
ICH3_LAN_RST_N
ICH3_RTCRST_N
SPST Switch
S8
PWR_BTN
Q68
Q67
NZT751
2N3904
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
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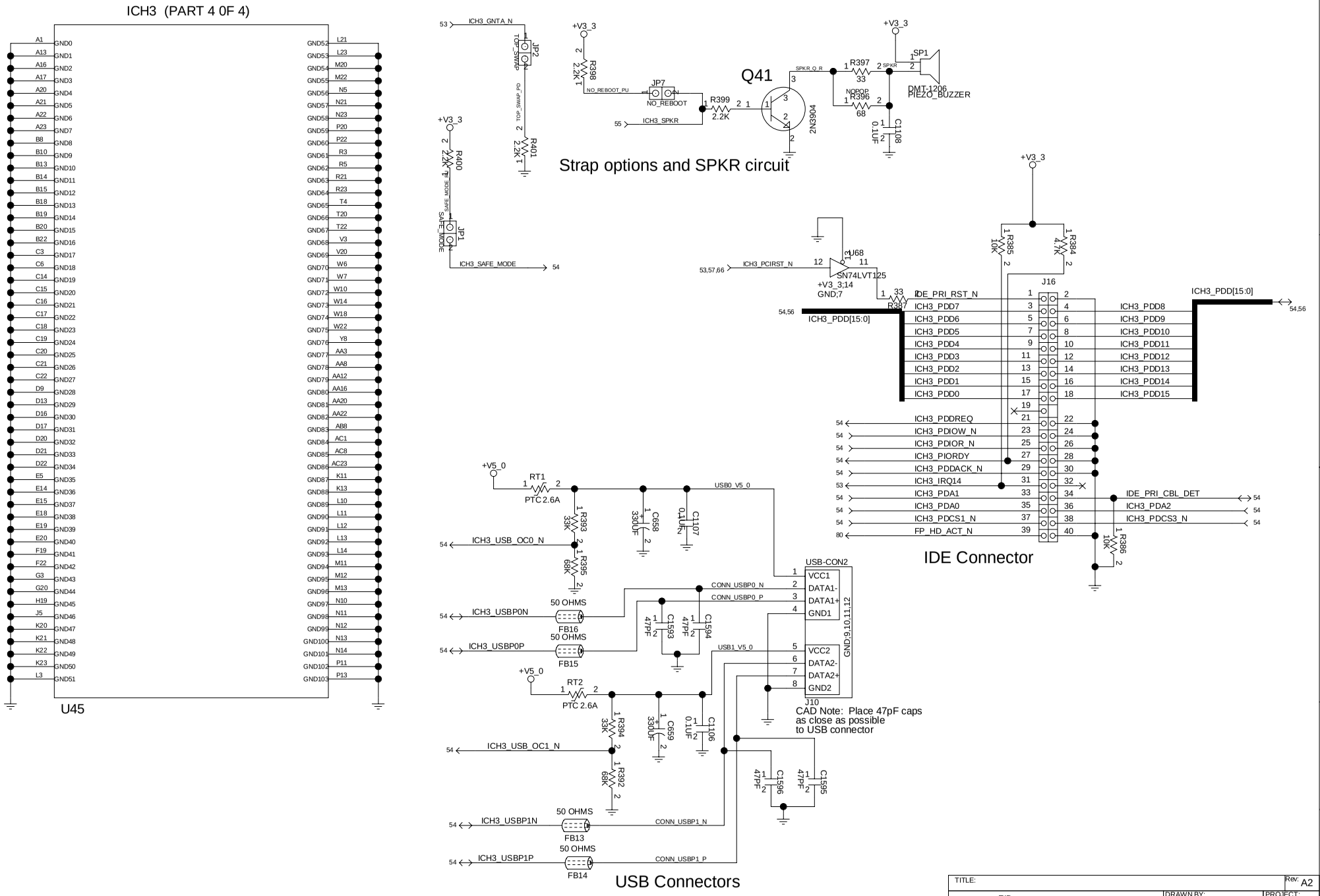
ICH3 (PART 4 0F 4)
U45
Strap options and SPKR circuit
ICH3_GNTA_N
JP2
TOP_SWAP
R398
2.2K
+V3_3
JP7
NO_REBOOT
NO_REBOOT_PU
R399
2.2K
ICH3_SPKR
Q41
2N3904
SPKR_Q_R
R397
33
SP1
SPKR
DMT-1206
PIEZO_BUZZER
R396
68
NOPOP
C1108
0.1UF
R401
2.2K
R400
2.2K
JP1
SAFE_MODE
ICH3_SAFE_MODE
ICH3_PCIRST_N
U68
SN74LVT125
+V3_3;14
GND;7
R385
10K
R384
4.7K
J16
IDE_PRI_RST_N
R387
33
ICH3_PDD[15:0]
ICH3_PDD7
ICH3_PDD6
ICH3_PDD5
ICH3_PDD4
ICH3_PDD3
ICH3_PDD2
ICH3_PDD1
ICH3_PDD0
ICH3_PDD8
ICH3_PDD9
ICH3_PDD10
ICH3_PDD11
ICH3_PDD12
ICH3_PDD13
ICH3_PDD14
ICH3_PDD15
ICH3_PDDREQ
ICH3_PDIOW_N
ICH3_PDIOR_N
ICH3_PIORDY
ICH3_PDDACK_N
ICH3_IRQ14
ICH3_PDA1
ICH3_PDA0
ICH3_PDCS1_N
FP_HD_ACT_N
IDE_PRI_CBL_DET
ICH3_PDA2
ICH3_PDCS3_N
R386
10K
IDE Connector
RT1
PTC 2.6A
USB0_V5_0
C658
330UF
C1107
0.1UF
R393
33K
R395
68K
ICH3_USB_OC0_N
ICH3_USBP0N
ICH3_USBP0P
50 OHMS
FB16
FB15
CONN_USBP0_N
CONN_USBP0_P
C1593
47PF
C1594
47PF
USB-CON2
VCC1
DATA1-
DATA1+
GND1
VCC2
DATA2-
DATA2+
GND2
GND;9,10,11,12
J10
USB1_V5_0
RT2
PTC 2.6A
R394
33K
C659
330UF
C1106
0.1UF
R392
68K
ICH3_USB_OC1_N
ICH3_USBP1N
ICH3_USBP1P
FB13
FB14
CONN_USBP1_N
CONN_USBP1_P
C1596
47PF
C1595
47PF
CAD Note: Place 47pF caps as close as possible to USB connector
USB Connectors
TITLE:
Rev: A2
EID
Chandler, Arizona
DRAWN BY: TCL
PROJECT: MC
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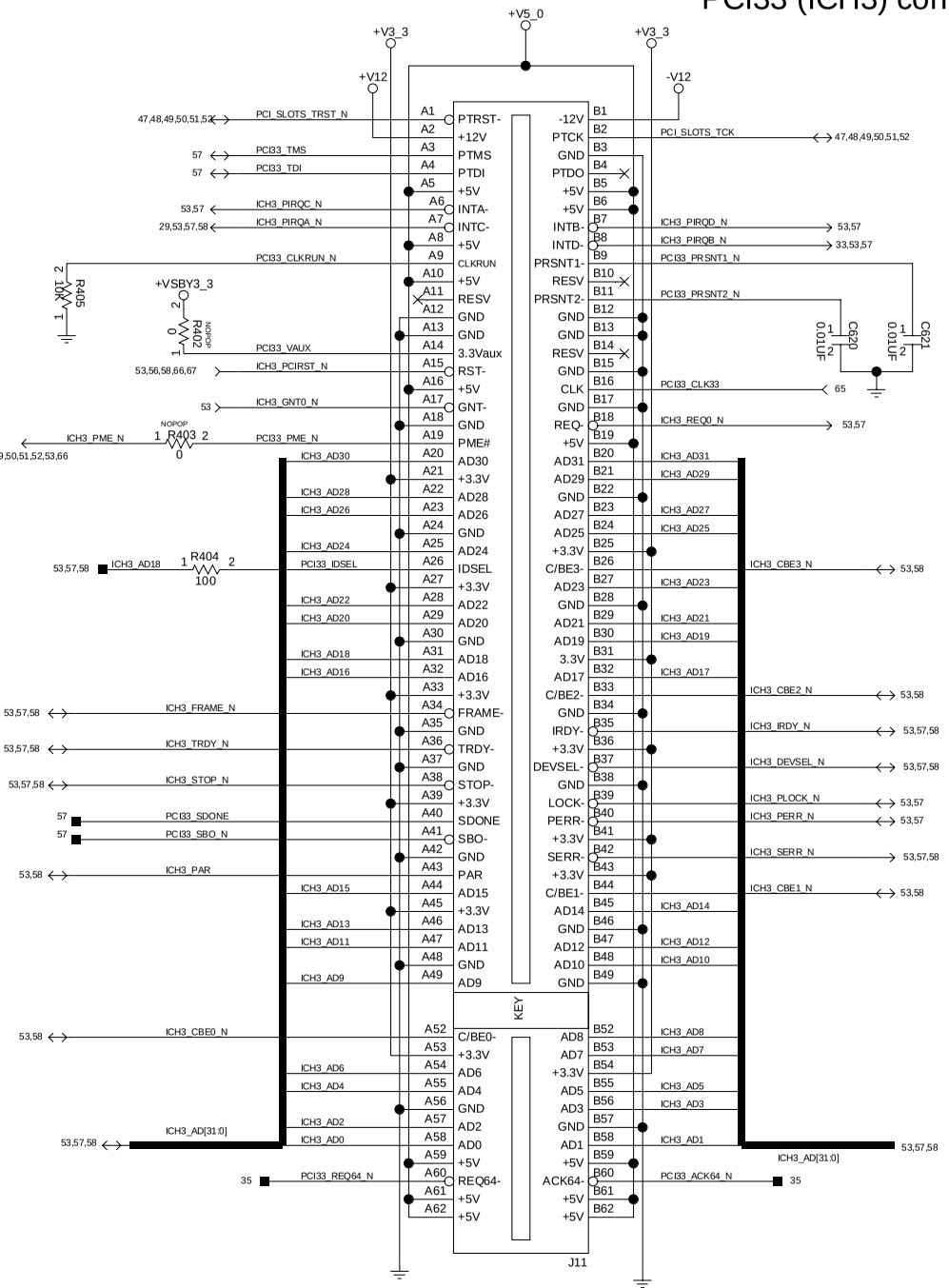
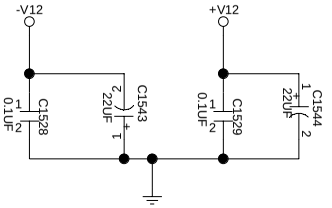
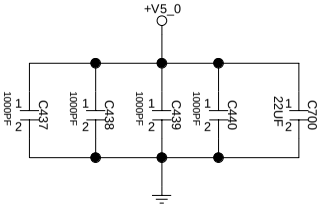
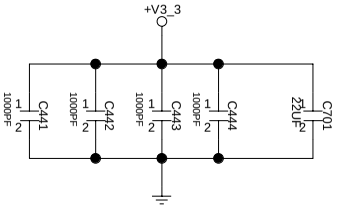
PCI33 (ICH3) connector, termination and decoupling

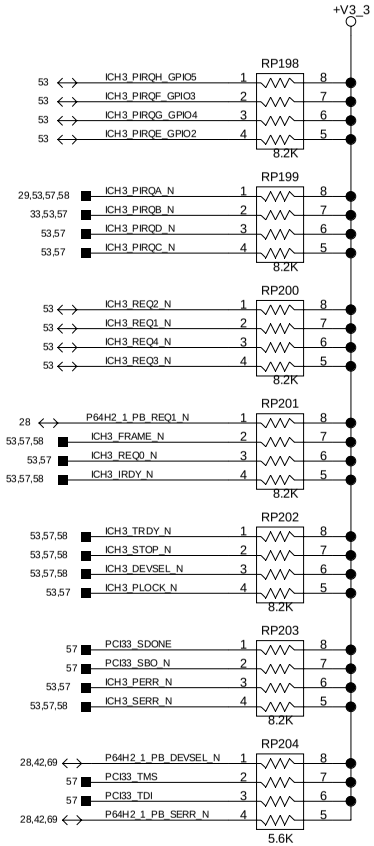






Place caps near connector





TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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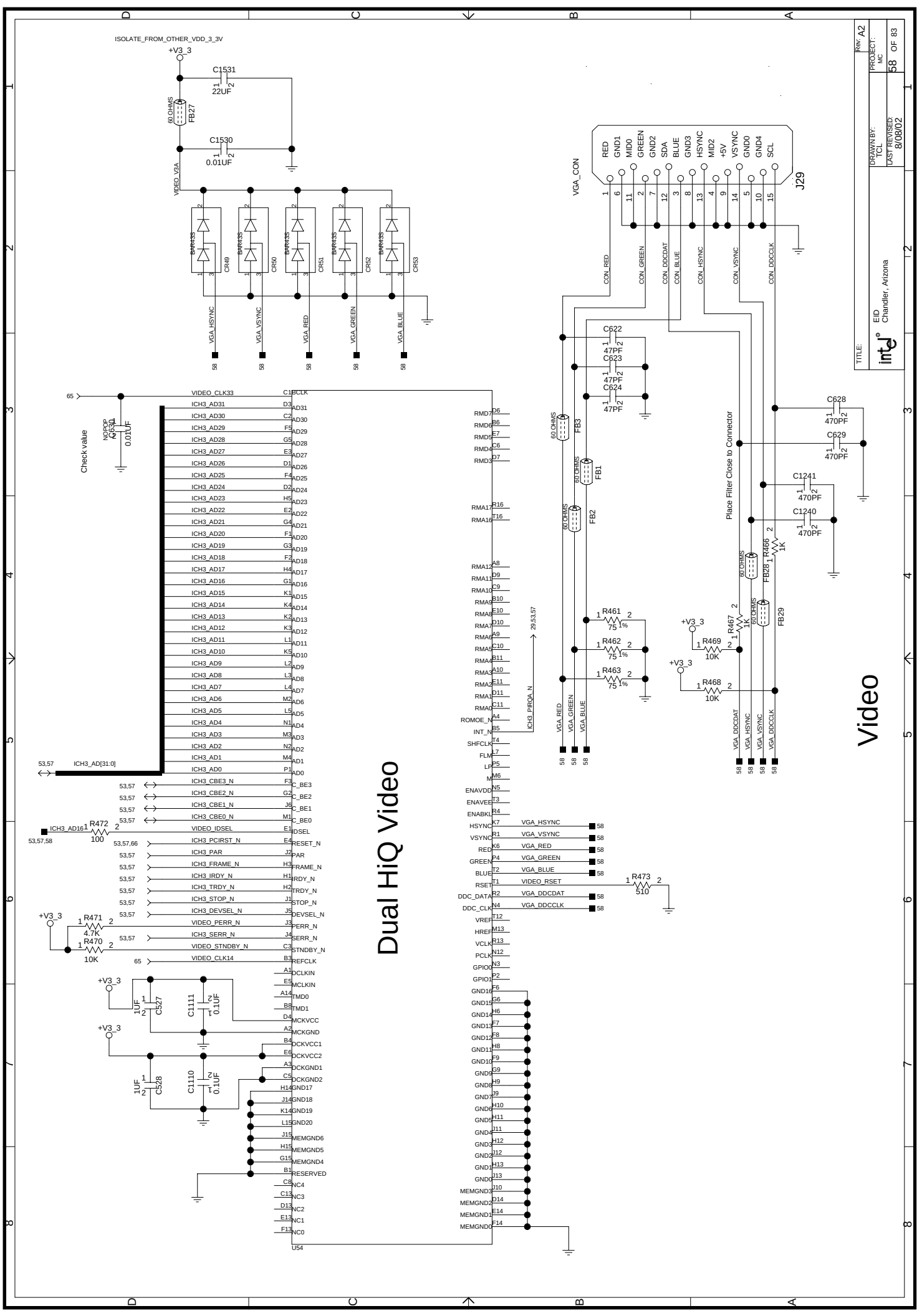
Video
Dual HiQ Video
ISOLATE_FROM_OTHER_VDD_3_3V
+V3_3
C1531
22UF
C1530
0.01UF
FB27
60 OHMS
VIDEO_V3A
BAR43S
CR49
CR50
CR51
CR52
CR53
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_CON
J29
RED
GND1
MID0
GREEN
GND2
SDA
BLUE
GND3
HSYNC
MID2
+5V
VSYNC
GND0
GND4
SCL
CON_RED
CON_GREEN
CON_DDCDAT
CON_BLUE
CON_HSYNC
CON_VSYNC
CON_DDCCLK
C622
C623
C624
47PF
FB3
FB1
FB2
C628
C629
C1241
C1240
470PF
Place Filter Close to Connector
R466
1K
FB28
FB29
R461
R462
R463
75 1%
R467
R469
R468
10K
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_DDCDAT
VGA_HSYNC
VGA_VSYNC
VGA_DDCCLK
Check value
NOPOP
C531
0.01UF
VIDEO_CLK33
ICH3_AD31
ICH3_AD30
ICH3_AD29
ICH3_AD28
ICH3_AD27
ICH3_AD26
ICH3_AD25
ICH3_AD24
ICH3_AD23
ICH3_AD22
ICH3_AD21
ICH3_AD20
ICH3_AD19
ICH3_AD18
ICH3_AD17
ICH3_AD16
ICH3_AD15
ICH3_AD14
ICH3_AD13
ICH3_AD12
ICH3_AD11
ICH3_AD10
ICH3_AD9
ICH3_AD8
ICH3_AD7
ICH3_AD6
ICH3_AD5
ICH3_AD4
ICH3_AD3
ICH3_AD2
ICH3_AD1
ICH3_AD0
ICH3_AD[31:0]
ICH3_CBE3_N
ICH3_CBE2_N
ICH3_CBE1_N
ICH3_CBE0_N
ICH3_AD16
R472
100
VIDEO_IDSEL
ICH3_PCIRST_N
ICH3_PAR
ICH3_FRAME_N
ICH3_IRDY_N
ICH3_TRDY_N
ICH3_STOP_N
ICH3_DEVSEL_N
VIDEO_PERR_N
ICH3_SERR_N
VIDEO_STNDBY_N
VIDEO_CLK14
R471
4.7K
R470
10K
C527
C528
C1111
C1110
0.1UF
U54
RMD7
RMD6
RMD5
RMD4
RMD3
RMA17
RMA16
RMA12
RMA11
RMA10
RMA9
RMA8
RMA7
RMA6
RMA5
RMA4
RMA3
RMA2
RMA1
RMA0
ROMOE_N
INT_N
SHFCLK
FLM
LP
M
ENAVDD
ENAVEE
ENABKL
HSYNC
VSYNC
RED
GREEN
BLUE
RSET
DDC_DATA
DDC_CLK
VREF
HREF
VCLK
PCLK
GPIO0
GPIO1
ICH3_PIRQA_N
VIDEO_RSET
VGA_DDCDAT
VGA_DDCCLK
R473
510
MEMGND3
MEMGND2
MEMGND1
MEMGND0
GND16
GND15
GND14
GND13
GND12
GND11
GND10
GND9
GND8
GND7
GND6
GND5
GND4
GND3
GND2
GND1
GND0
MCKVCC
MCKGND
DCKVCC1
DCKVCC2
DCKGND1
DCKGND2
GND17
GND18
GND19
GND20
MEMGND6
MEMGND5
MEMGND4
RESERVED
NC4
NC3
NC2
NC1
NC0
TITLE:
intel
EID
Chandler, Arizona
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TCL
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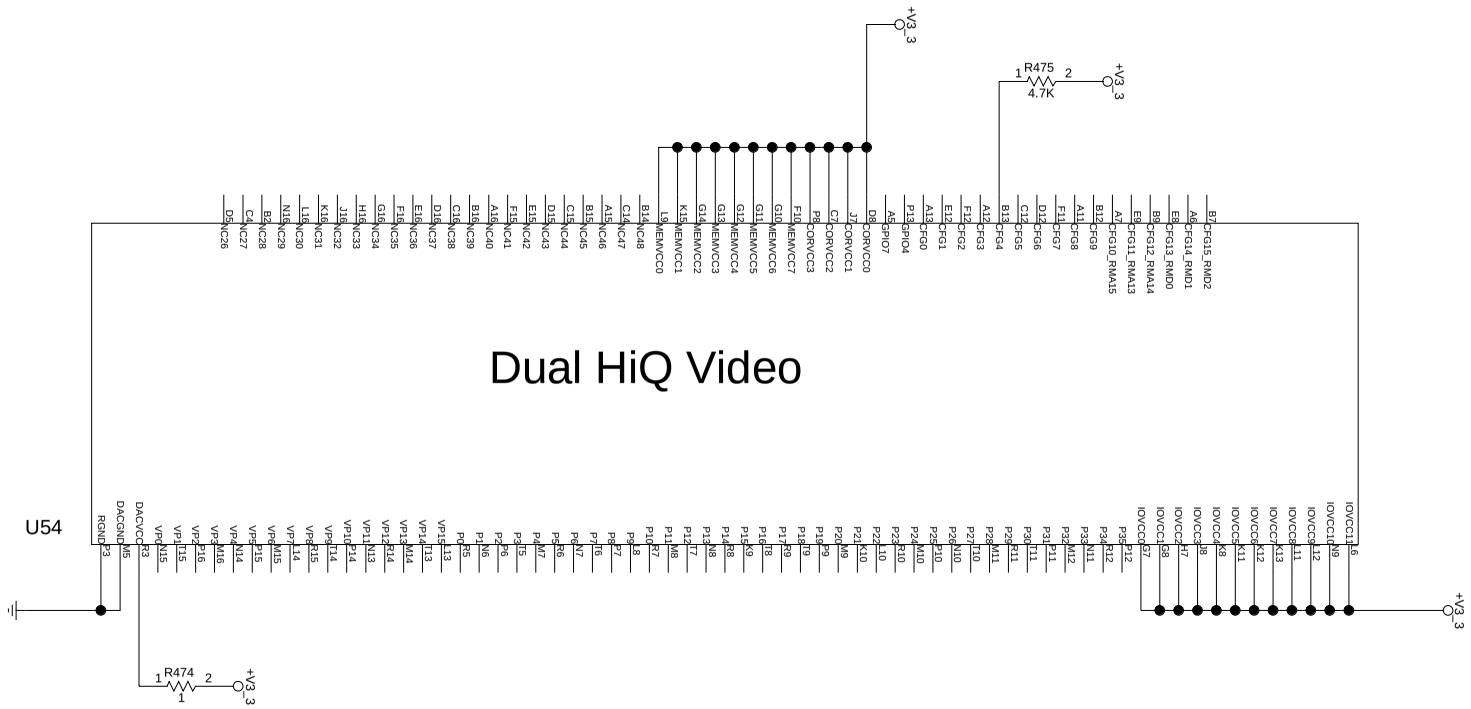

Video

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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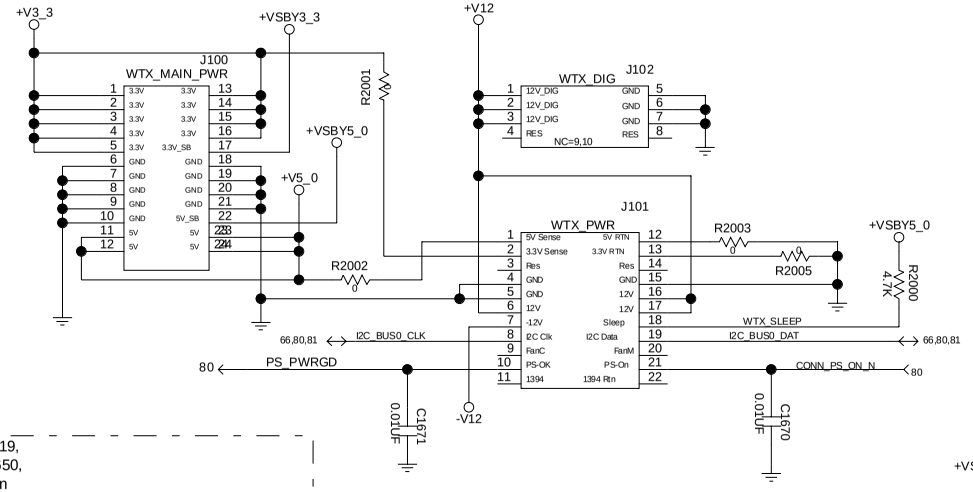
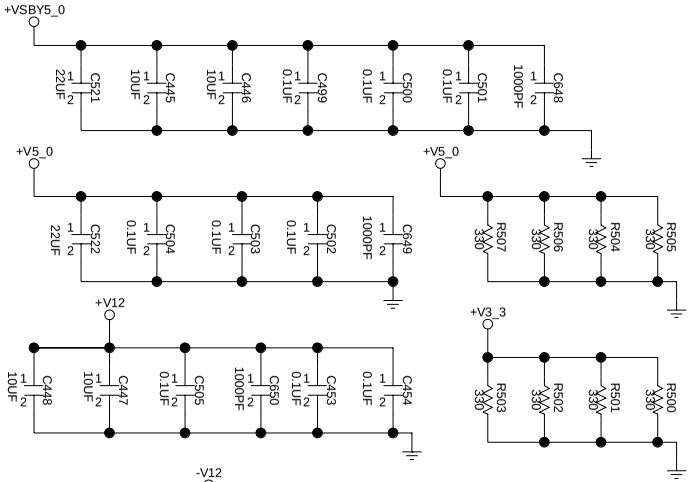
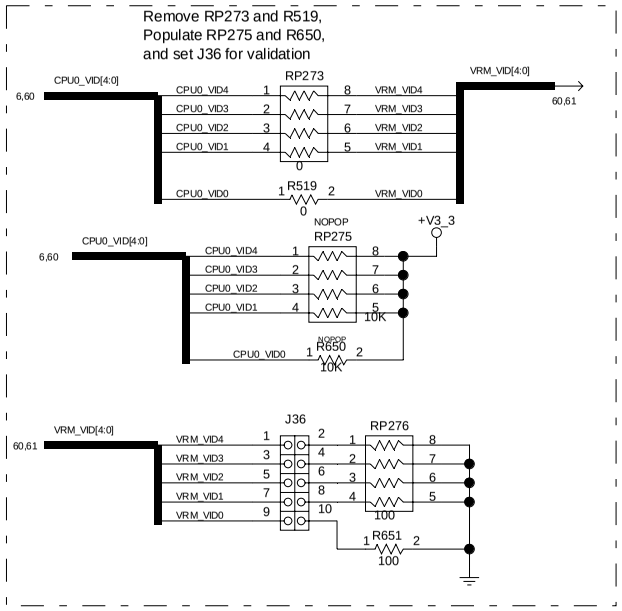
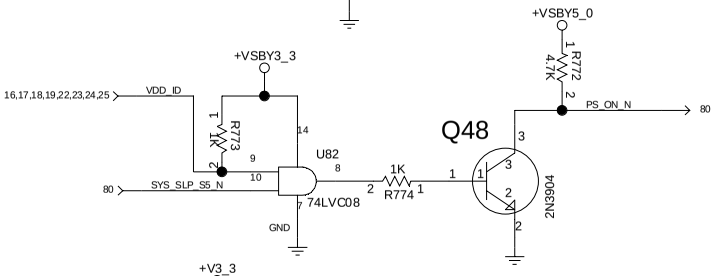
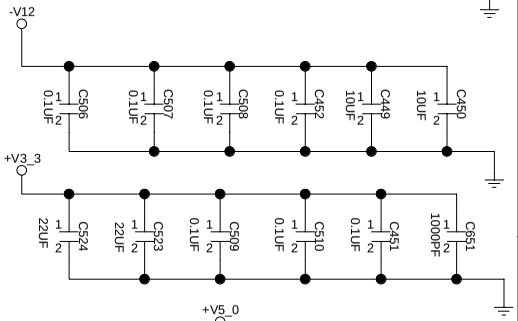
Power Connectors

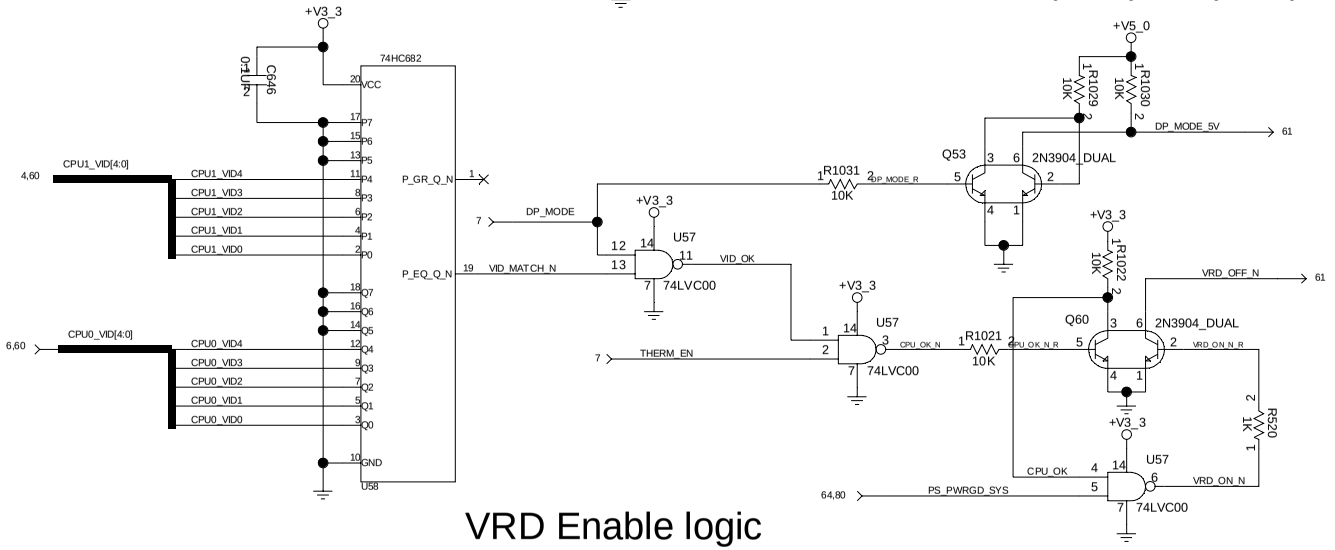






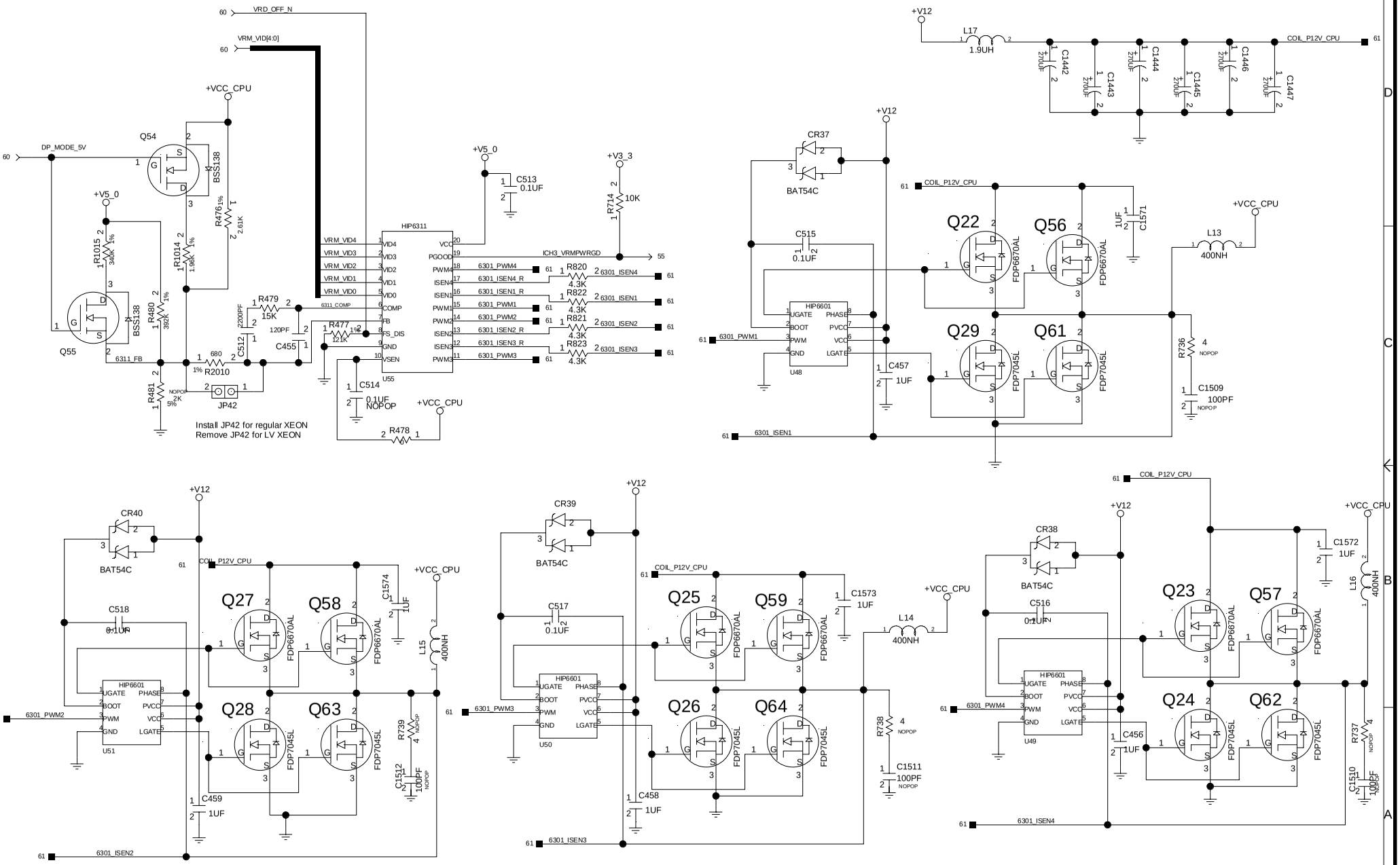






VRD Enable logic

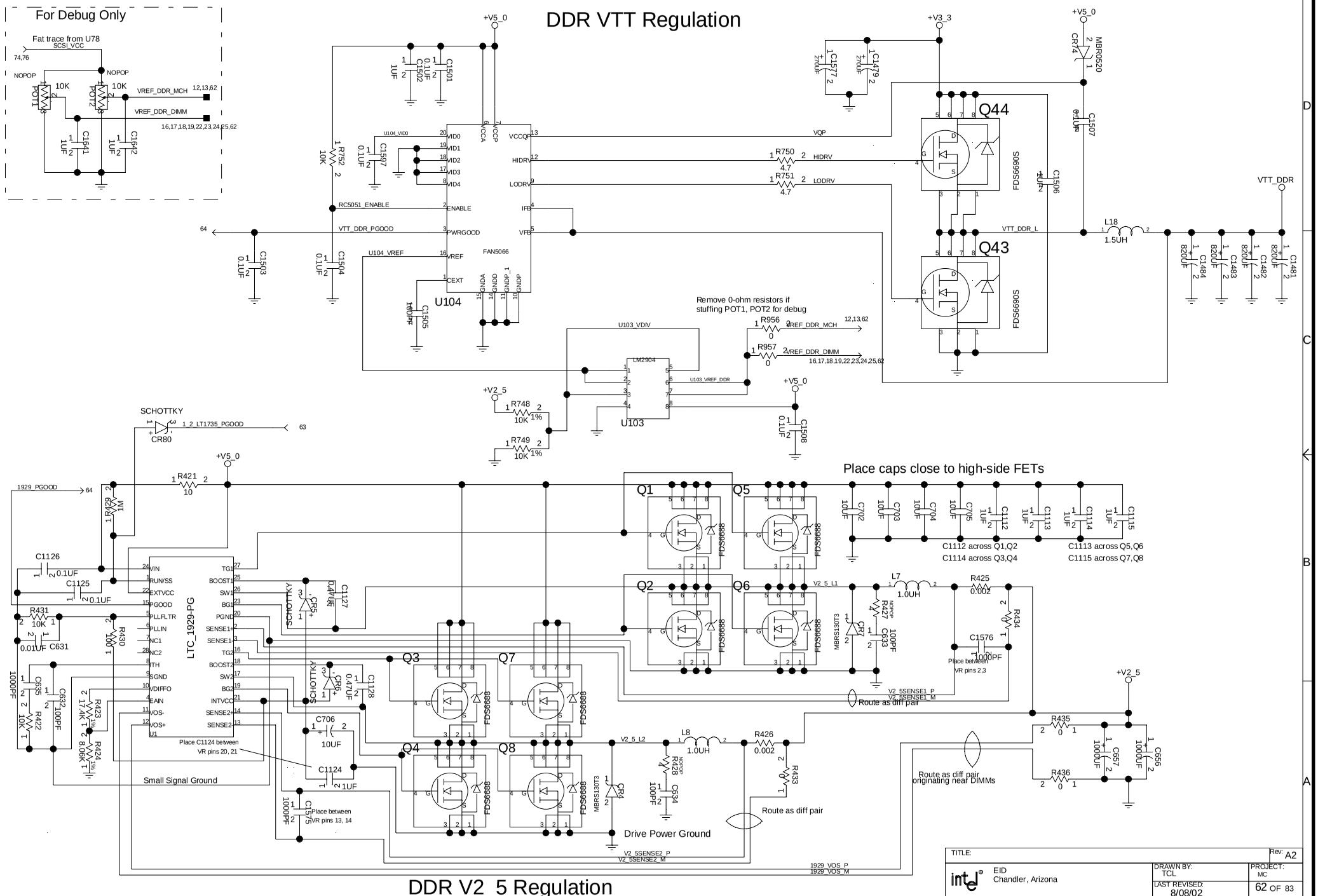
TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	60 OF 83	



Processor Voltage Regulator circuitry

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	61 OF 83

DDR VTT Regulation



DDR V2_5 Regulation

TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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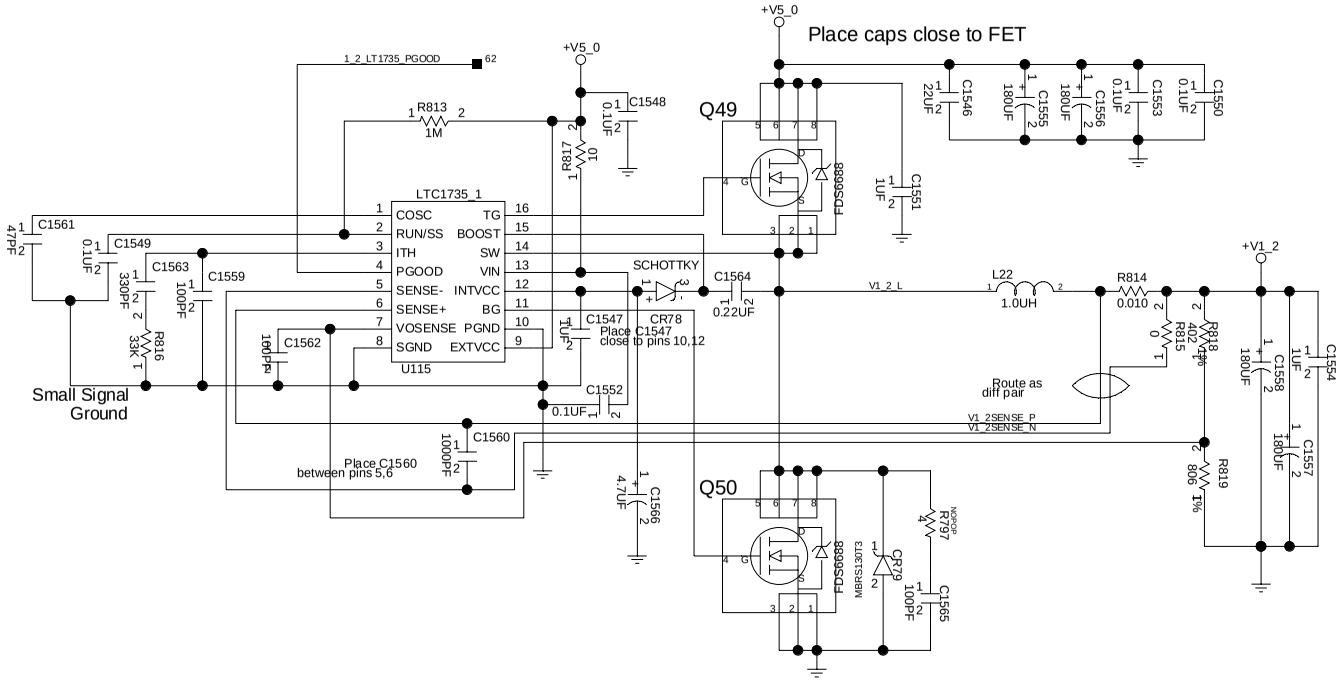
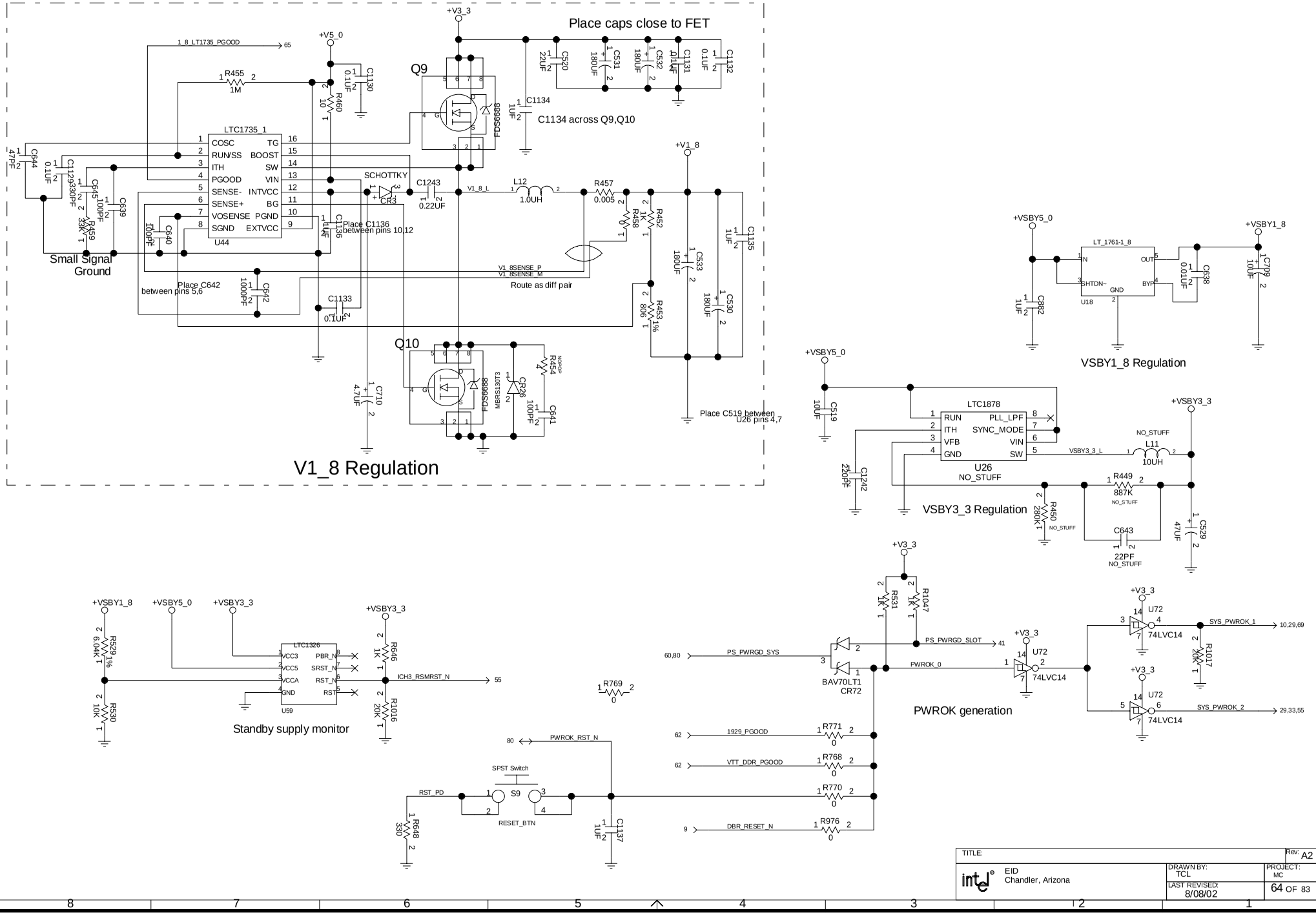
V1.2 Regulation



TITLE:			Rev: A2
intel EID Chandler, Arizona		DRAWN BY: TCL	PROJECT: MC
		LAST REVISED: 8/08/02	63 OF 83



TITLE:	Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL
	PROJECT: MC
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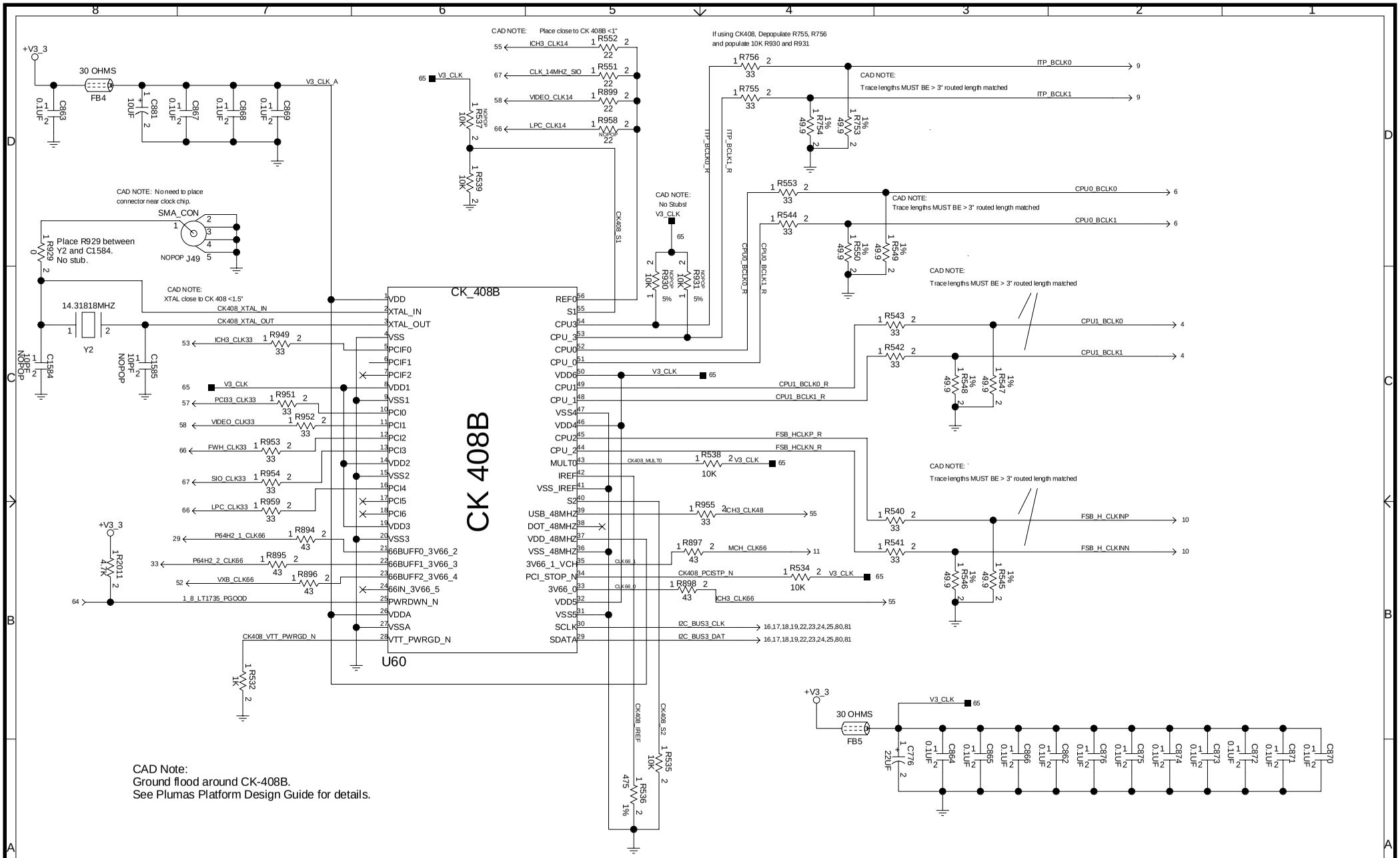
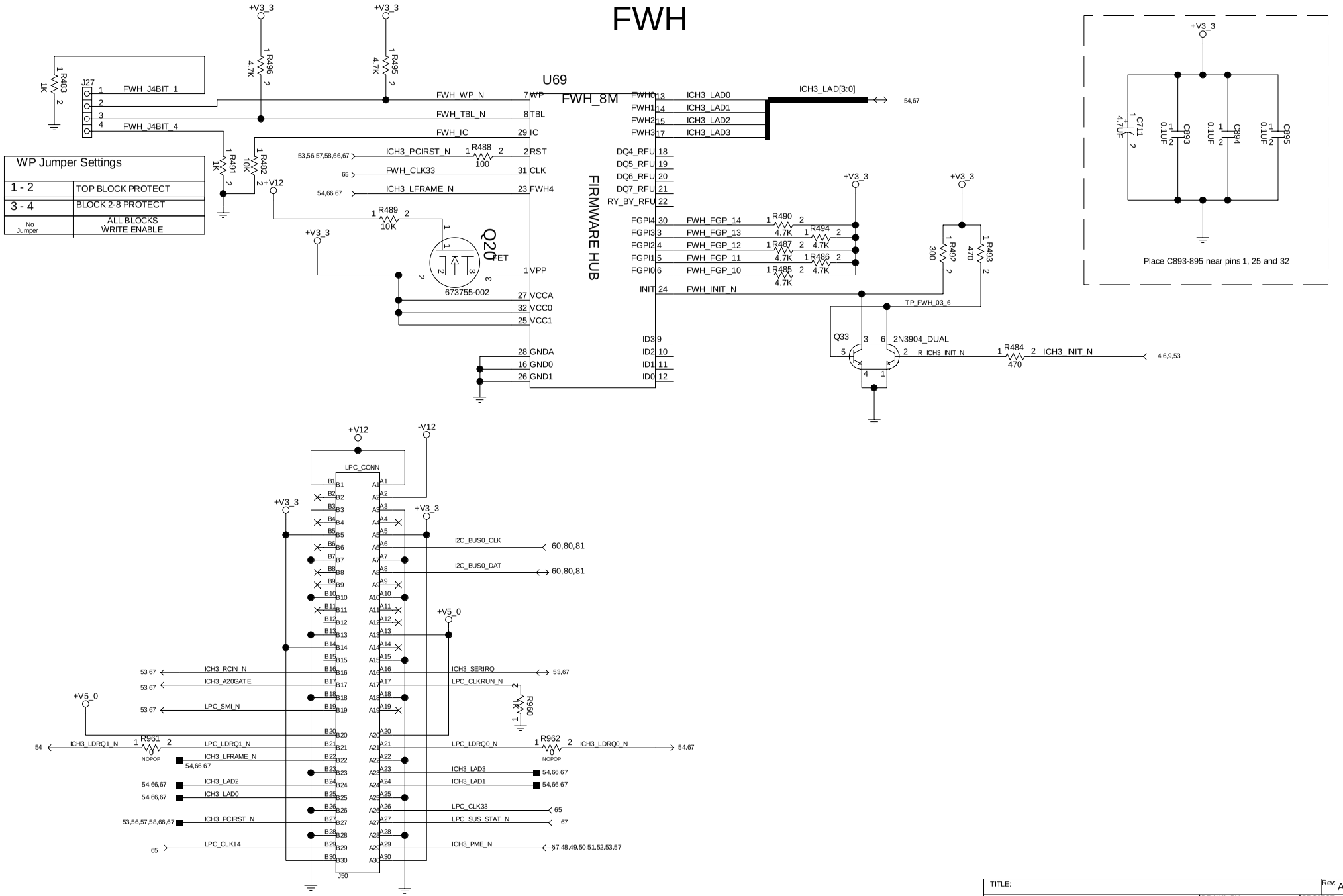


CK408-B
Clock Synthesizer

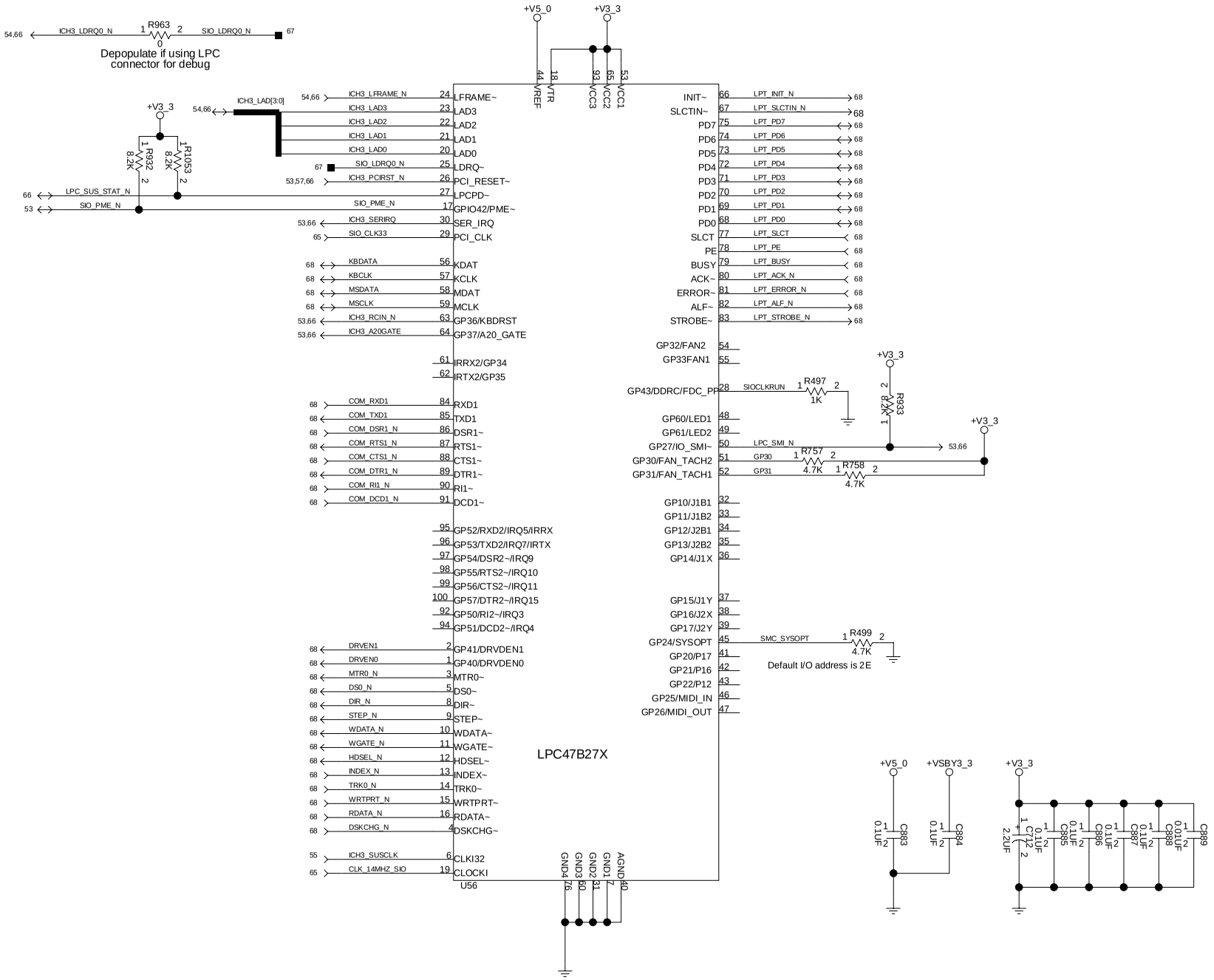
TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
	LAST REVISED: 8/08/02	65 OF 83

FWH



LPC connector (for debug only)

TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	66 OF 83	



SIO

TITLE:			Rev: A2
intel EID Chandler, Arizona		DRAWN BY: TCL	PROJECT: MC
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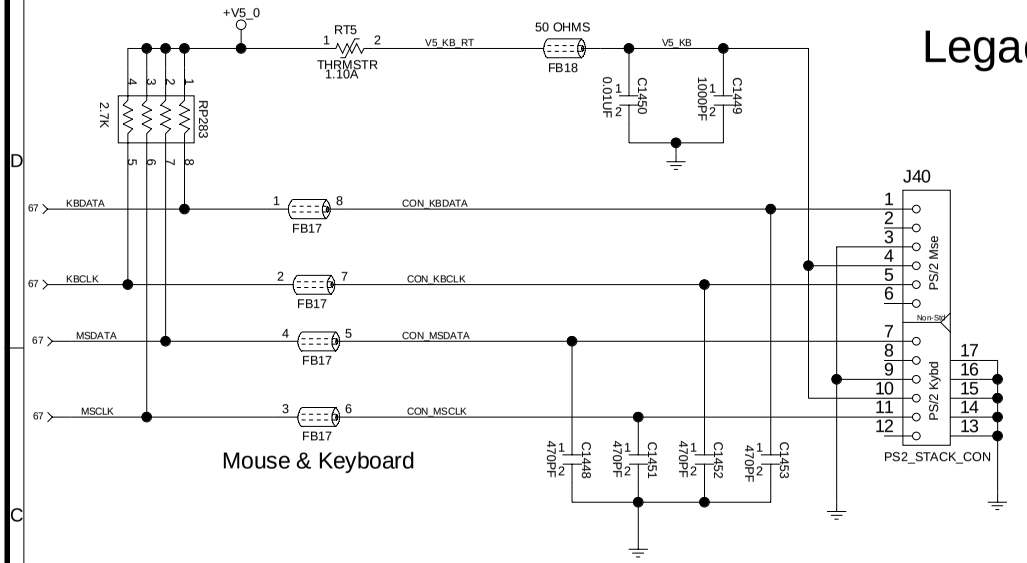
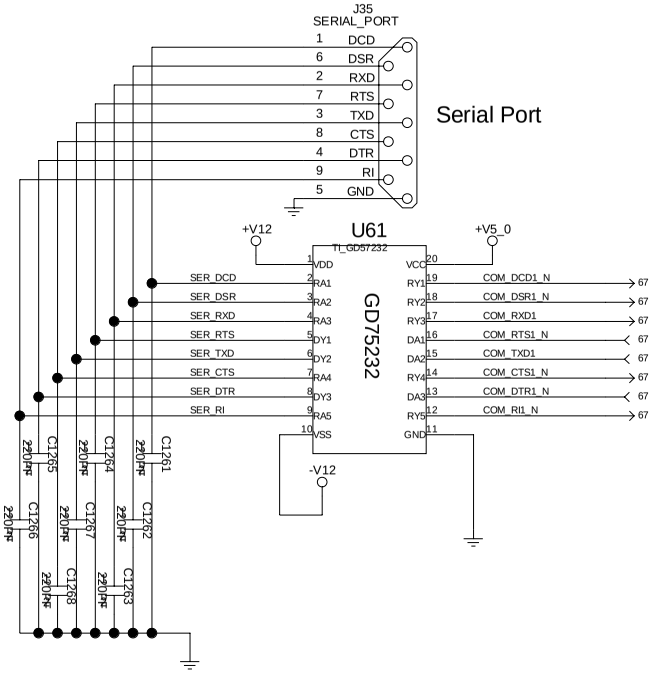
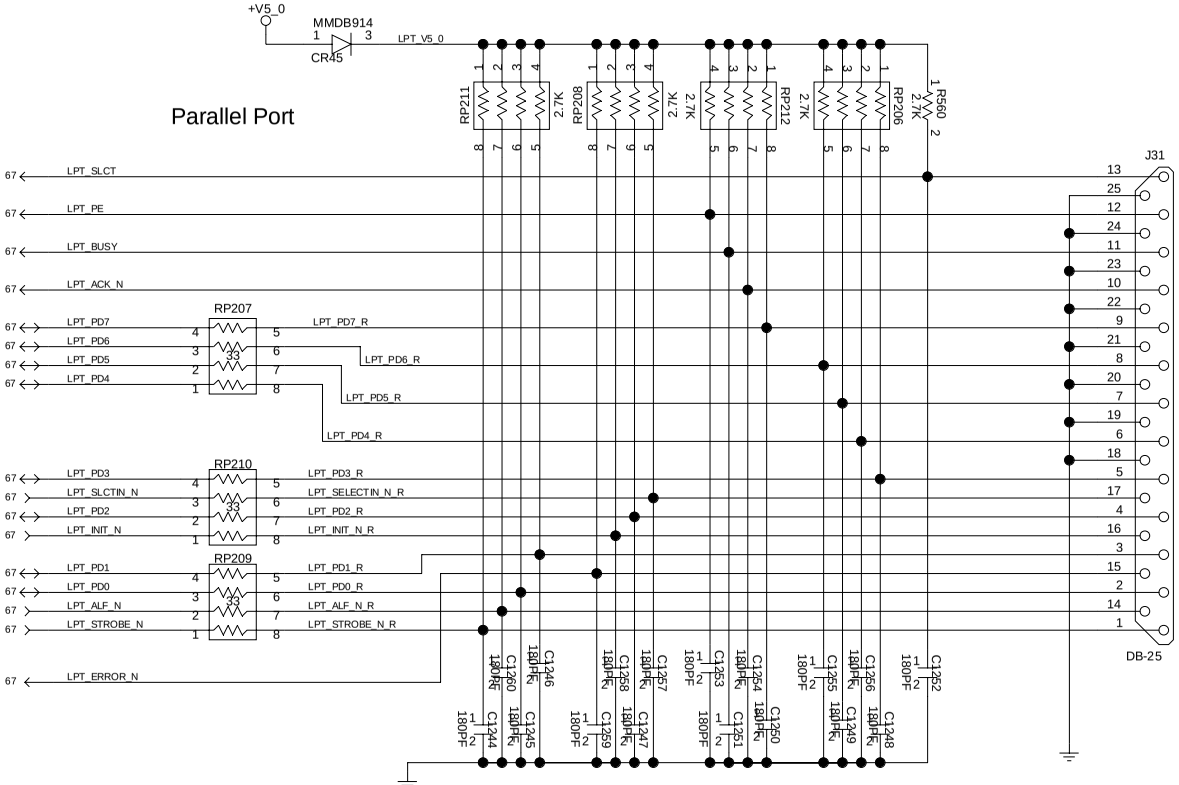
Legacy I/O



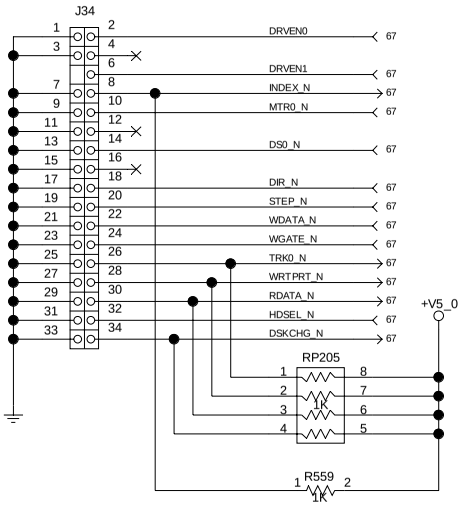
Mouse & Keyboard



Serial Port

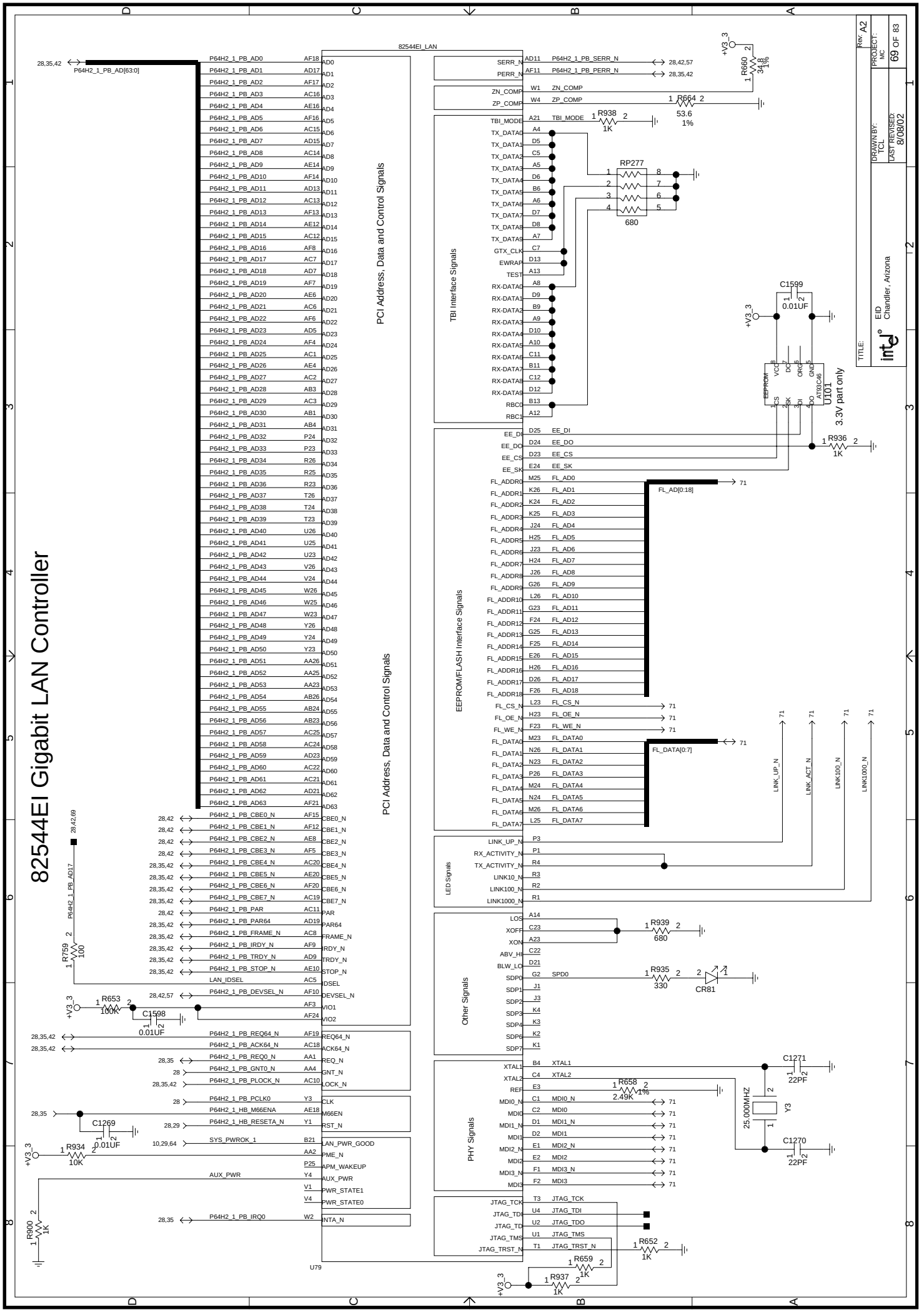


Parallel Port

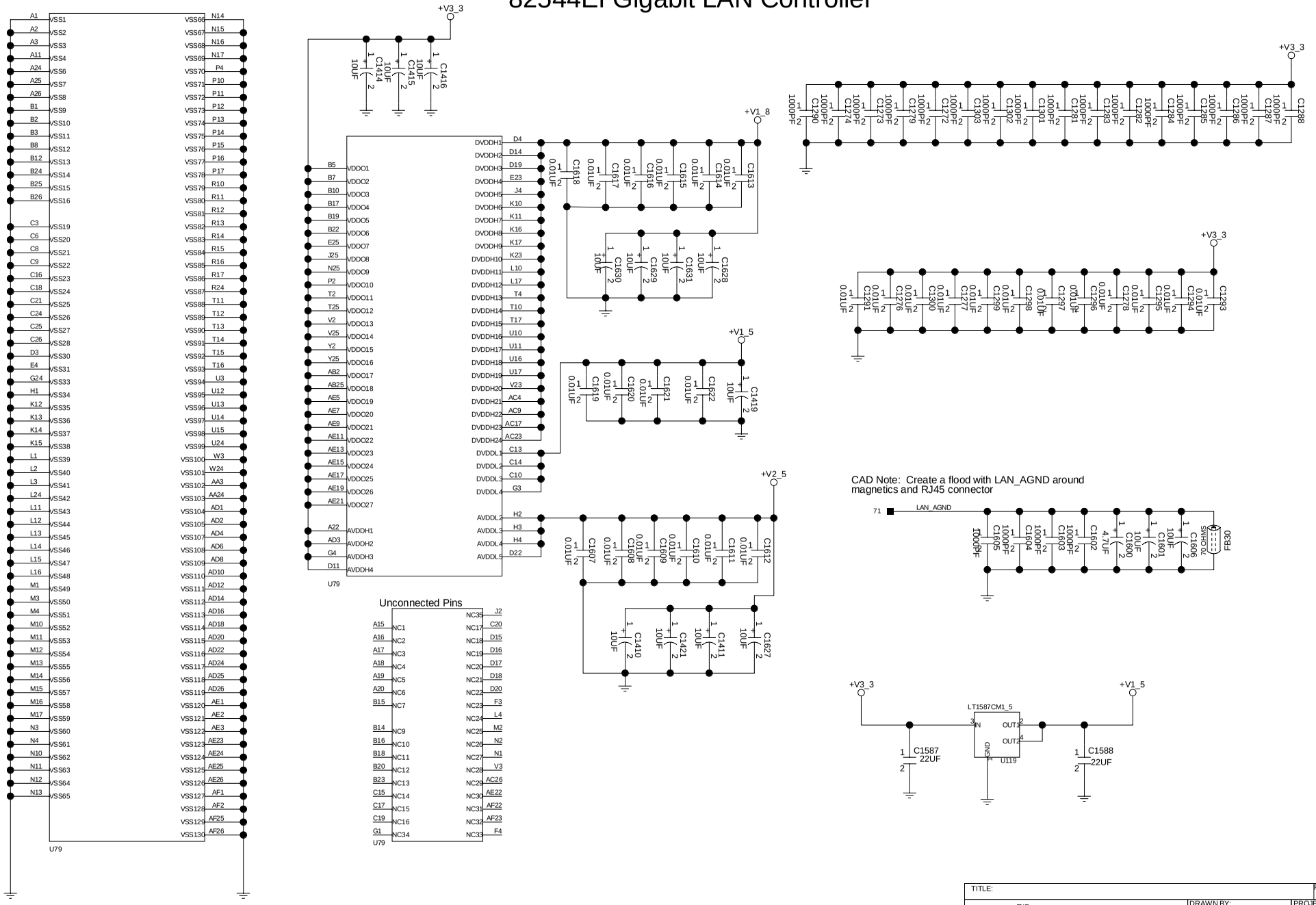


Floppy Connector

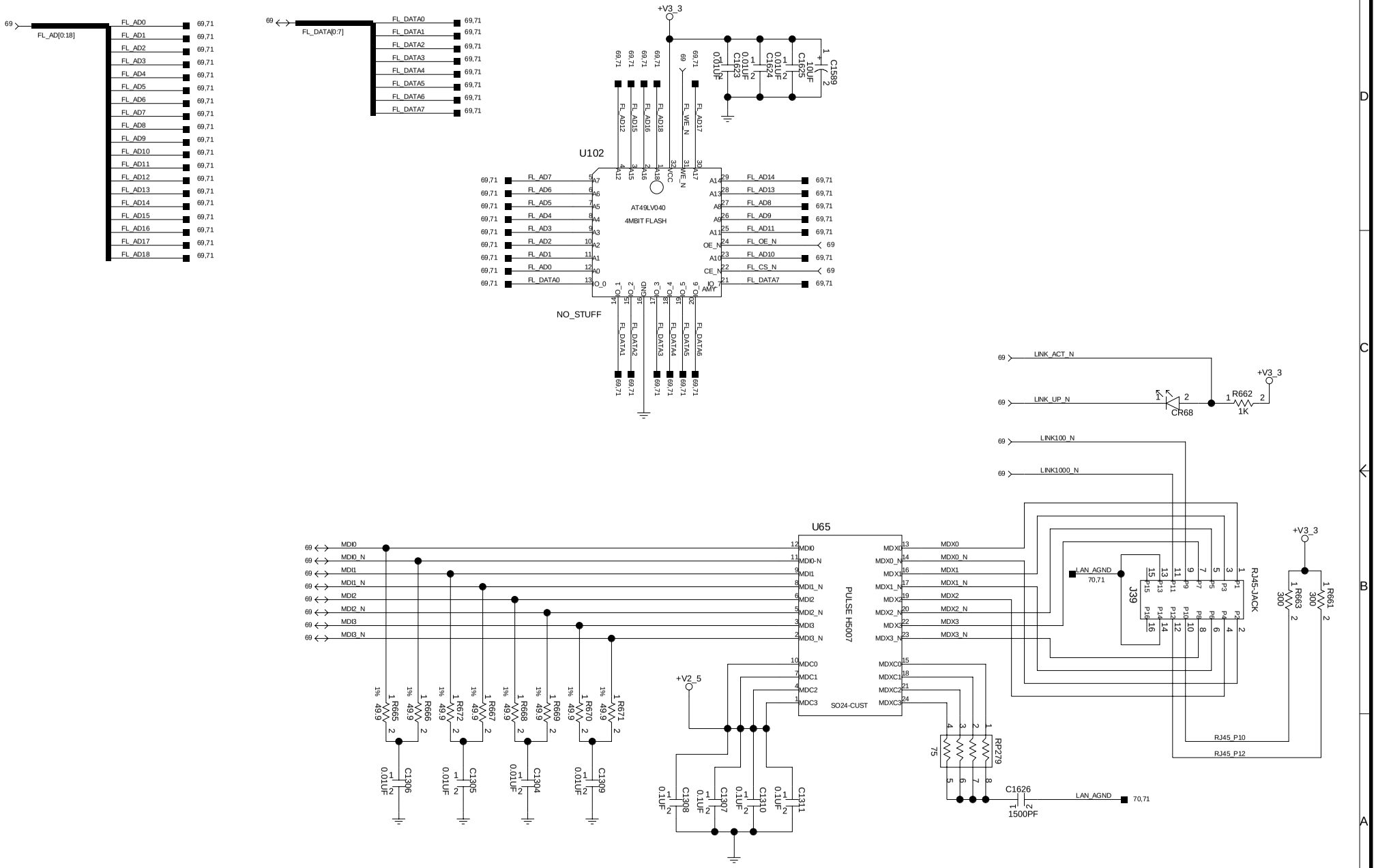
TITLE:		Rev: A2	
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	68 OF 83	


82544EI Gigabit LAN Controller
82544EI_LAN
PCI Address, Data and Control Signals
TBI Interface Signals
EEPROM/FLASH Interface Signals
LED Signals
Other Signals
PHY Signals
U79
U101
3.3V part only
P64H2_1_PB_AD[63:0]
FL_AD[0:18]
FL_DATA[0:7]
LINK_UP_N
LINK_ACT_N
LINK100_N
LINK1000_N
Rev: A2
PROJECT: MC
69 OF 83
DRAWN BY: TCL
LAST REVISED: 8/08/02
TITLE:
EID
Chandler, Arizona

82544EI Gigabit LAN Controller

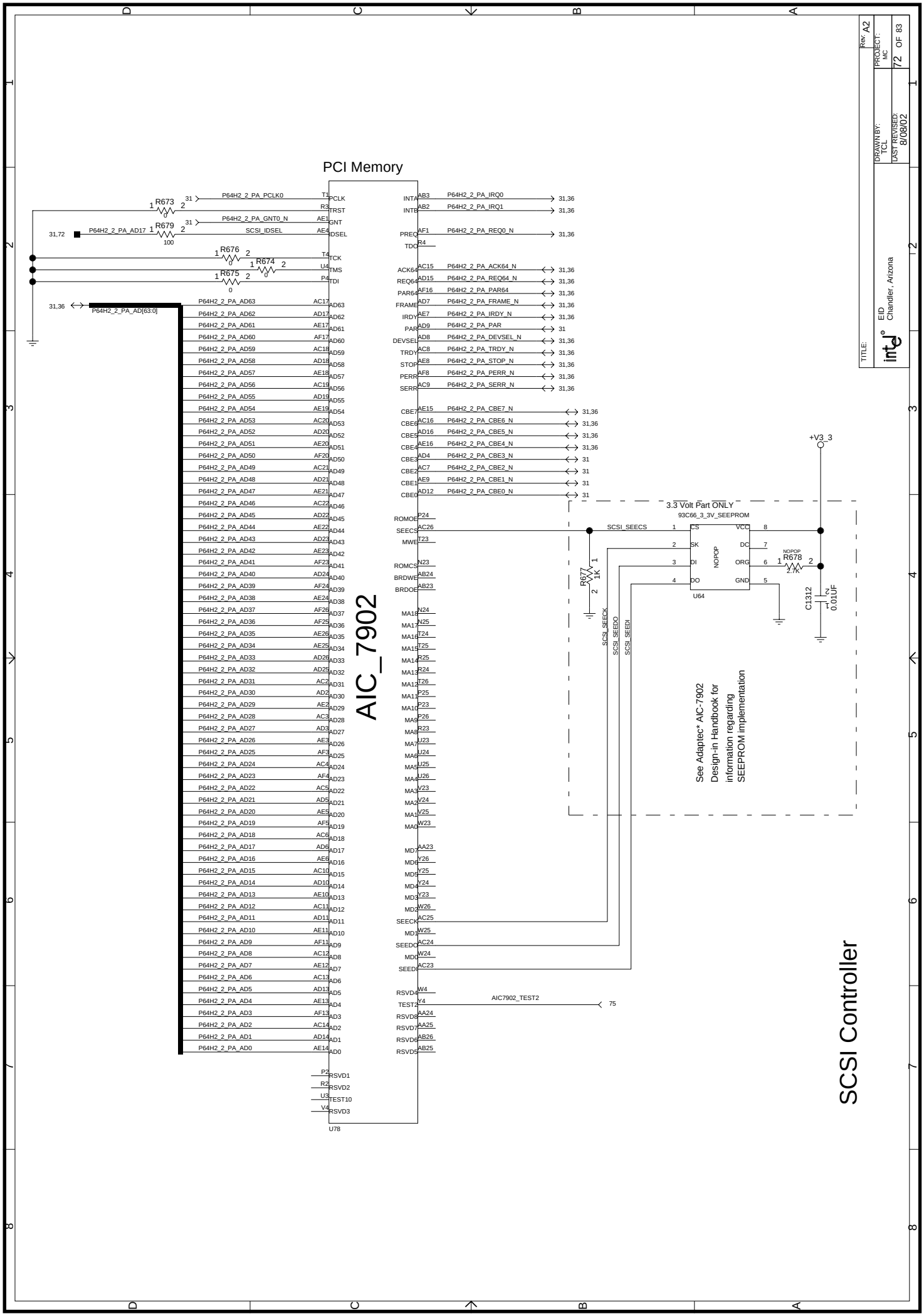


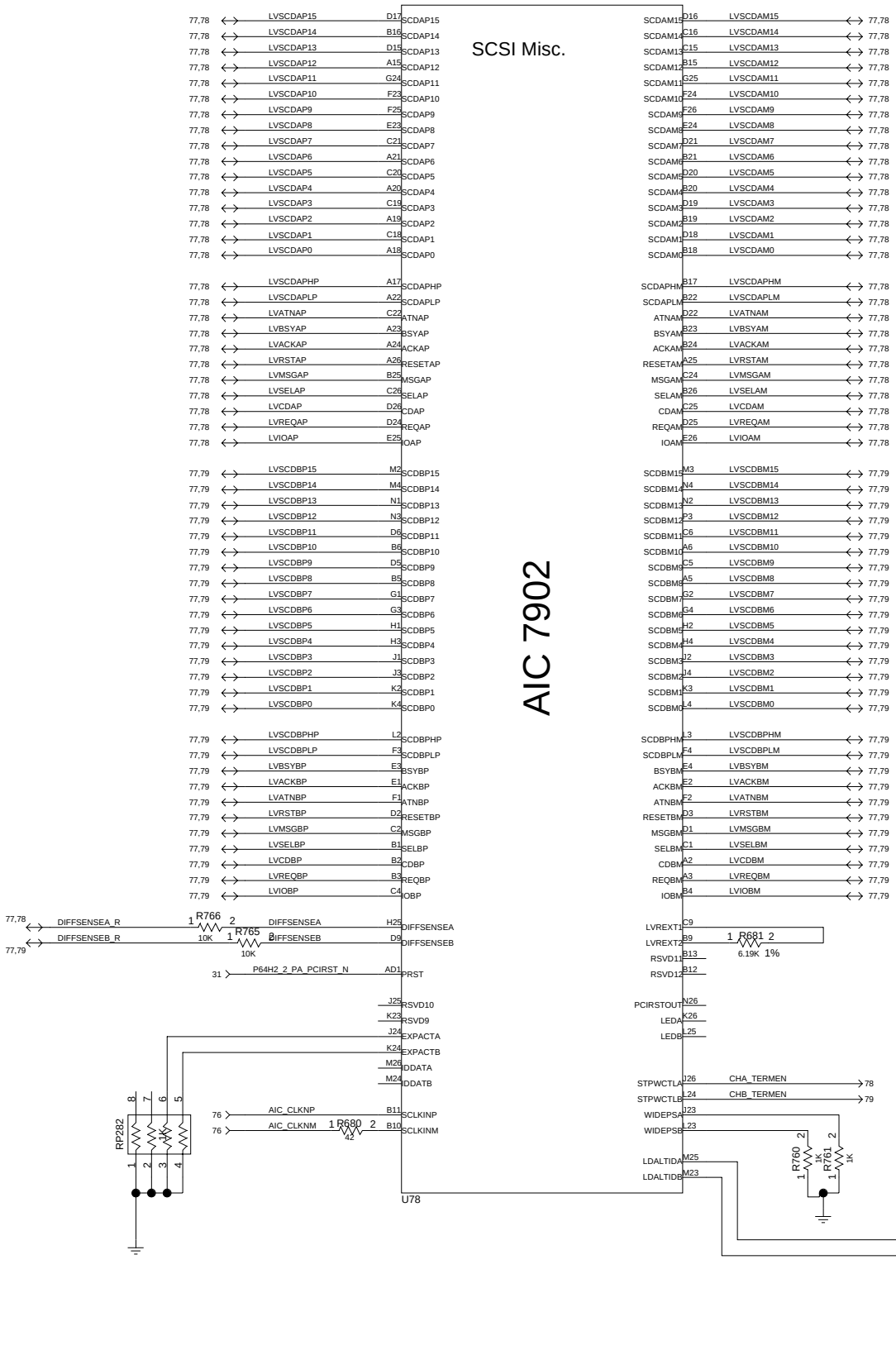
TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	70 OF 83	



LAN EEPROM, Magnetics and Connector

TITLE:	Rev: A2
EID Chandler, Arizona	DRAWN BY: TCL PROJECT: MC LAST REVISED: 8/08/02 71 OF 83


PCI Memory
AIC_7902
SCSI Controller
U78
P64H2_2_PA_PCLK0
P64H2_2_PA_GNT0_N
P64H2_2_PA_AD17
SCSI_IDSEL
P64H2_2_PA_AD[63:0]
R673
R679
R676
R674
R675
100
P64H2_2_PA_IRQ0
P64H2_2_PA_IRQ1
P64H2_2_PA_REQ0_N
P64H2_2_PA_ACK64_N
P64H2_2_PA_REQ64_N
P64H2_2_PA_PAR64
P64H2_2_PA_FRAME_N
P64H2_2_PA_IRDY_N
P64H2_2_PA_PAR
P64H2_2_PA_DEVSEL_N
P64H2_2_PA_TRDY_N
P64H2_2_PA_STOP_N
P64H2_2_PA_PERR_N
P64H2_2_PA_SERR_N
P64H2_2_PA_CBE7_N
P64H2_2_PA_CBE6_N
P64H2_2_PA_CBE5_N
P64H2_2_PA_CBE4_N
P64H2_2_PA_CBE3_N
P64H2_2_PA_CBE2_N
P64H2_2_PA_CBE1_N
P64H2_2_PA_CBE0_N
3.3 Volt Part ONLY
93C66_3_3V_SEEPROM
SCSI_SEECS
SCSI_SEECK
SCSI_SEEDO
SCSI_SEEDI
R677
1K
R678
2.7K
NOPOP
C1312
0.01UF
U64
+V3_3
See Adaptec* AIC-7902 Design-in Handbook for information regarding SEEPROM implementation
AIC7902_TEST2
Rev: A2
PROJECT: MC
SHEET 72 OF 83
DRAWN BY: TCL
LAST REVISED: 8/08/02
TITLE:
EID
Chandler, Arizona



TITLE:	Rev: A2
intel EID Chandler, Arizona	PROJECT: MC
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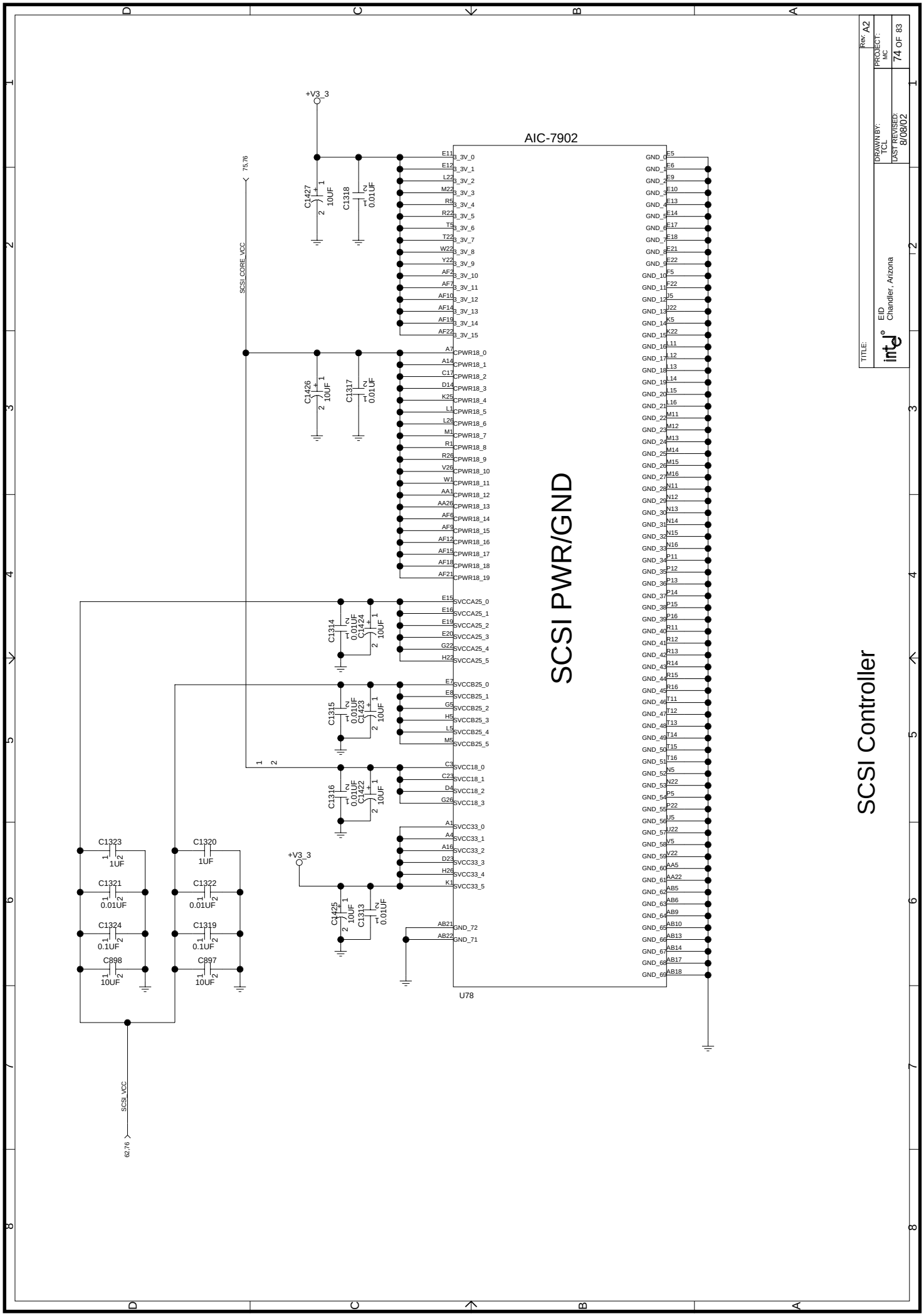
LAST REVISED: 8/08/02	


AIC-7902
SCSI PWR/GND
SCSI Controller
U78
+V3_3
SCSI_CORE_VCC
SCSI_VCC
75,76
62,76
C1427 10UF
C1318 0.01UF
C1426 10UF
C1317 0.01UF
C1314 0.01UF
C1424 10UF
C1315 0.01UF
C1423 10UF
C1316 0.01UF
C1422 10UF
C1425 10UF
C1313 0.01UF
C1323 1UF
C1320 1UF
C1321 0.01UF
C1322 0.01UF
C1324 0.1UF
C1319 0.1UF
C898 10UF
C897 10UF
3_3V_0
3_3V_1
3_3V_2
3_3V_3
3_3V_4
3_3V_5
3_3V_6
3_3V_7
3_3V_8
3_3V_9
3_3V_10
3_3V_11
3_3V_12
3_3V_13
3_3V_14
3_3V_15
CPWR18_0
CPWR18_1
CPWR18_2
CPWR18_3
CPWR18_4
CPWR18_5
CPWR18_6
CPWR18_7
CPWR18_8
CPWR18_9
CPWR18_10
CPWR18_11
CPWR18_12
CPWR18_13
CPWR18_14
CPWR18_15
CPWR18_16
CPWR18_17
CPWR18_18
CPWR18_19
SVCCA25_0
SVCCA25_1
SVCCA25_2
SVCCA25_3
SVCCA25_4
SVCCA25_5
SVCCB25_0
SVCCB25_1
SVCCB25_2
SVCCB25_3
SVCCB25_4
SVCCB25_5
SVCC18_0
SVCC18_1
SVCC18_2
SVCC18_3
SVCC33_0
SVCC33_1
SVCC33_2
SVCC33_3
SVCC33_4
SVCC33_5
GND_72
GND_71
GND_0
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
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GND_64
GND_65
GND_66
GND_67
GND_68
GND_69
TITLE:
Rev: A2
PROJECT: MC
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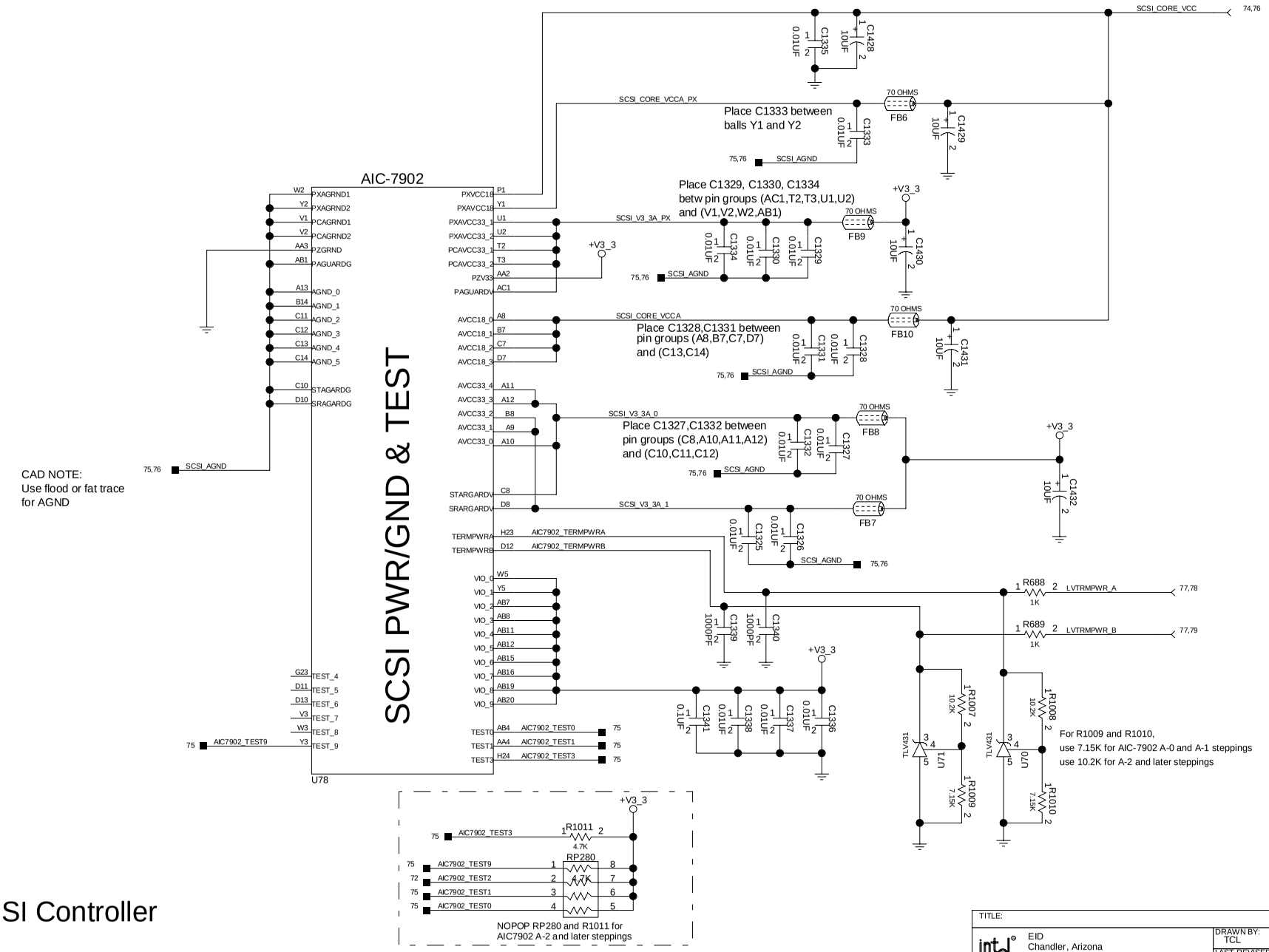
DRAWN BY: TCL
LAST REVISED: 8/08/02
EID Chandler, Arizona



SCSI Controller

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intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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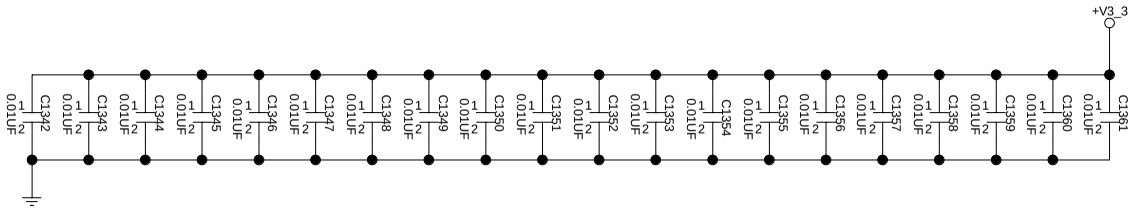
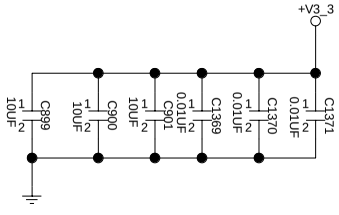
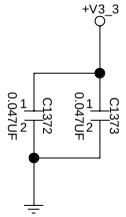
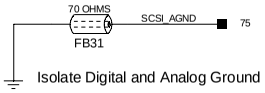
AIC-7902 SCSI Decoupling

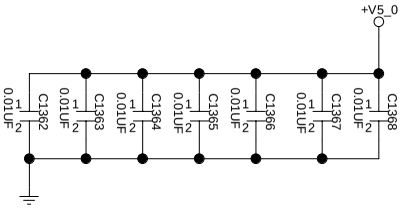




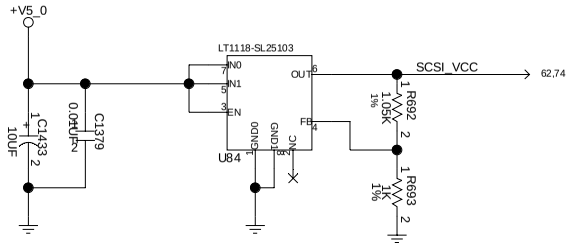


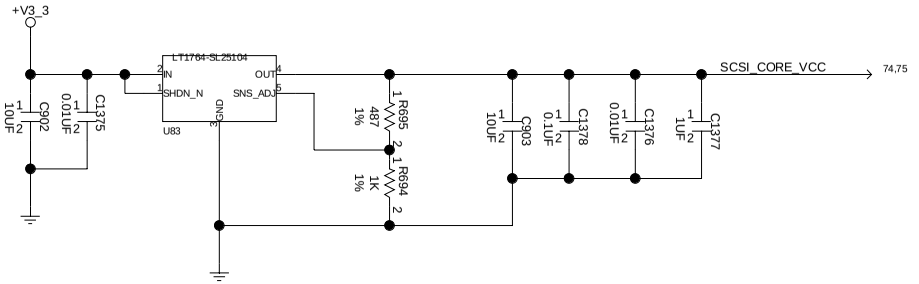
CAD NOTE:
Use flood or fat trace
for SCSI_AGND

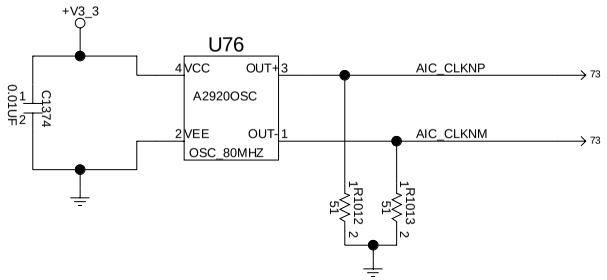




Voltage Regulators and SCSI Clock







TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
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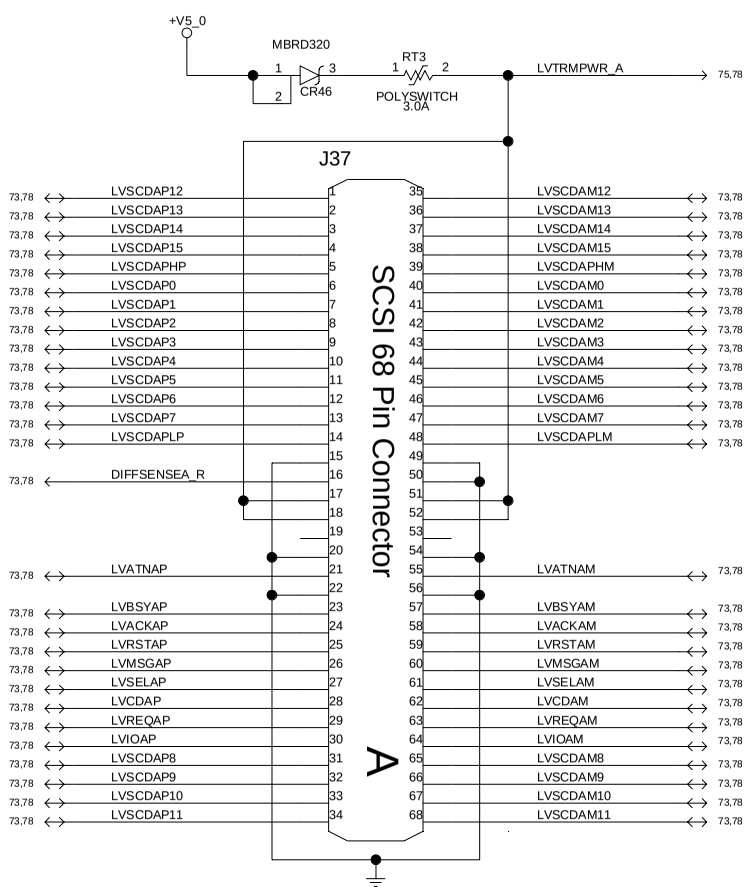
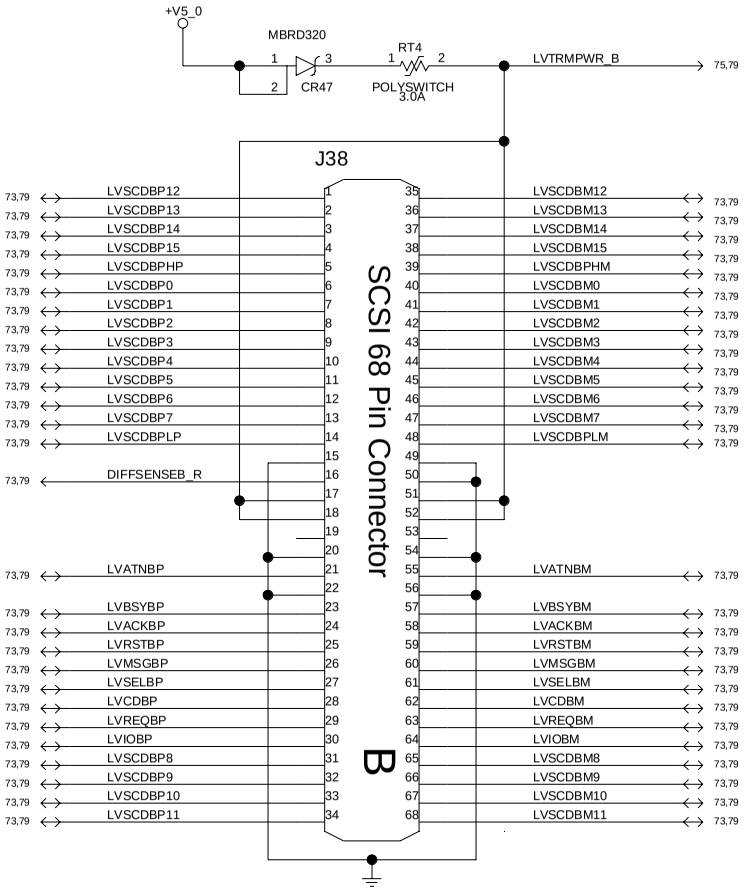
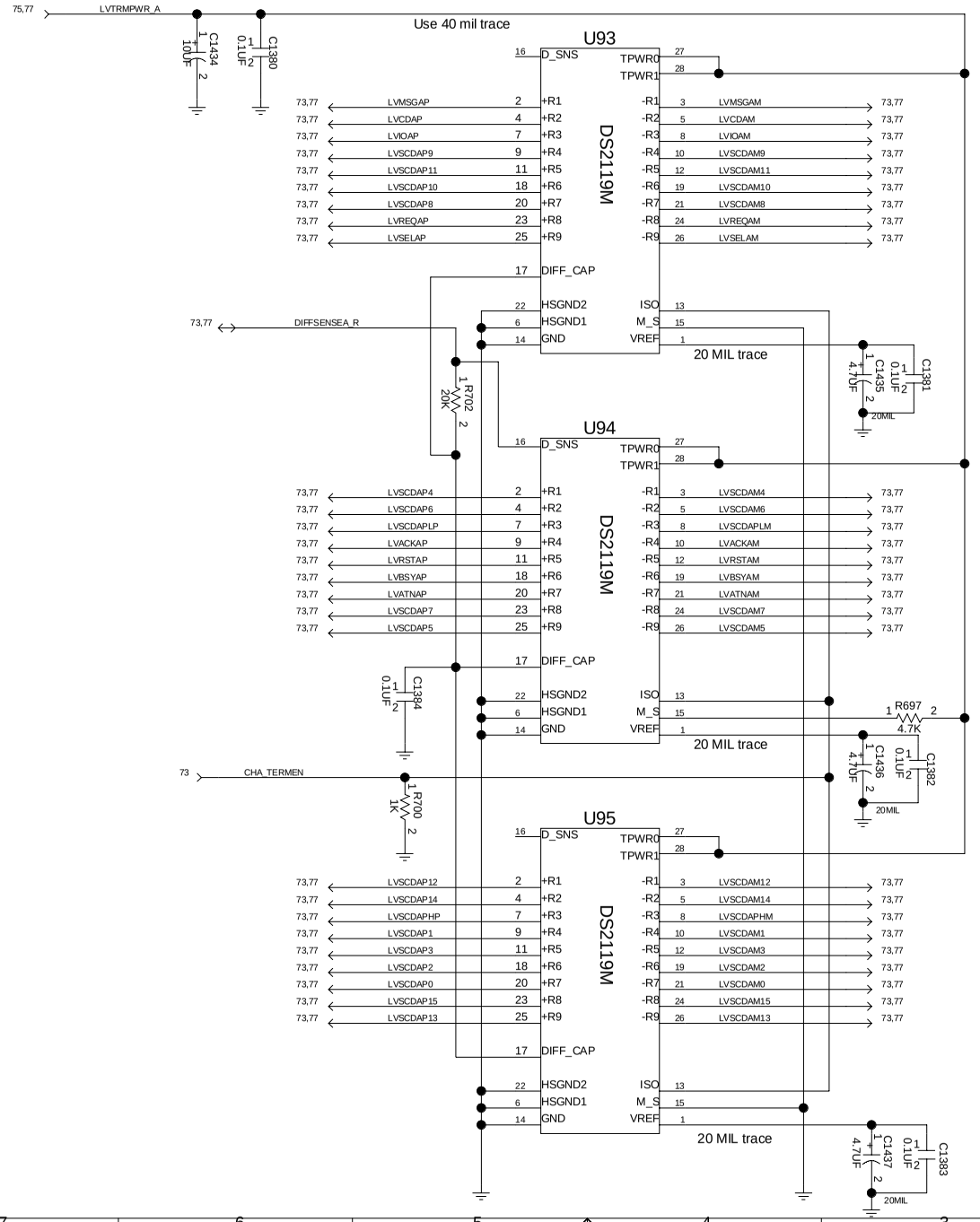
SCSI Connectors A and B





TITLE:			Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC	
	LAST REVISED: 8/08/02	77 OF 83	

LVD/SE Termination for SCSI Channel A



TITLE:		Rev: A2
intel EID Chandler, Arizona	DRAWN BY: TCL	PROJECT: MC
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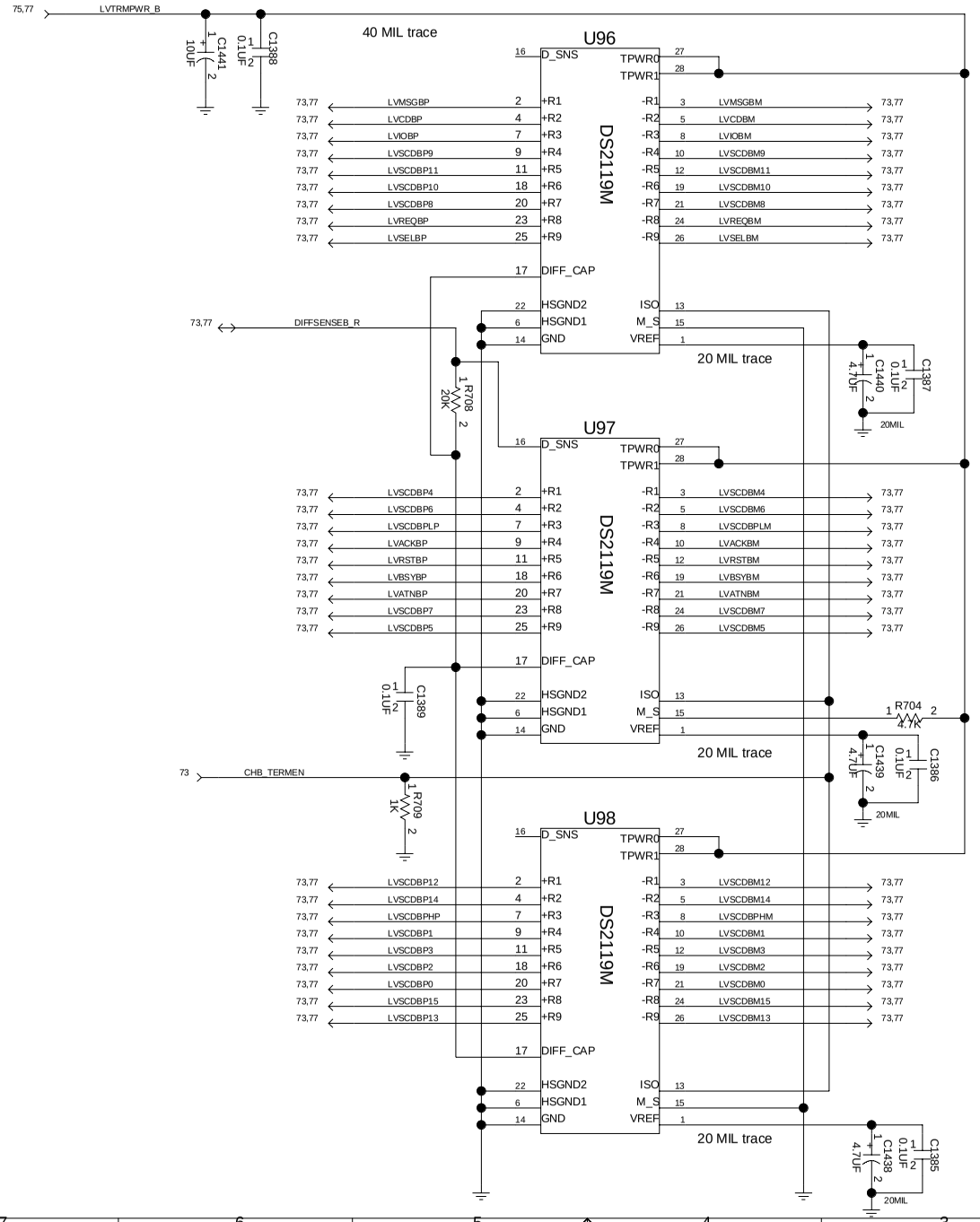
LVD/SE Termination for SCSI Channel B



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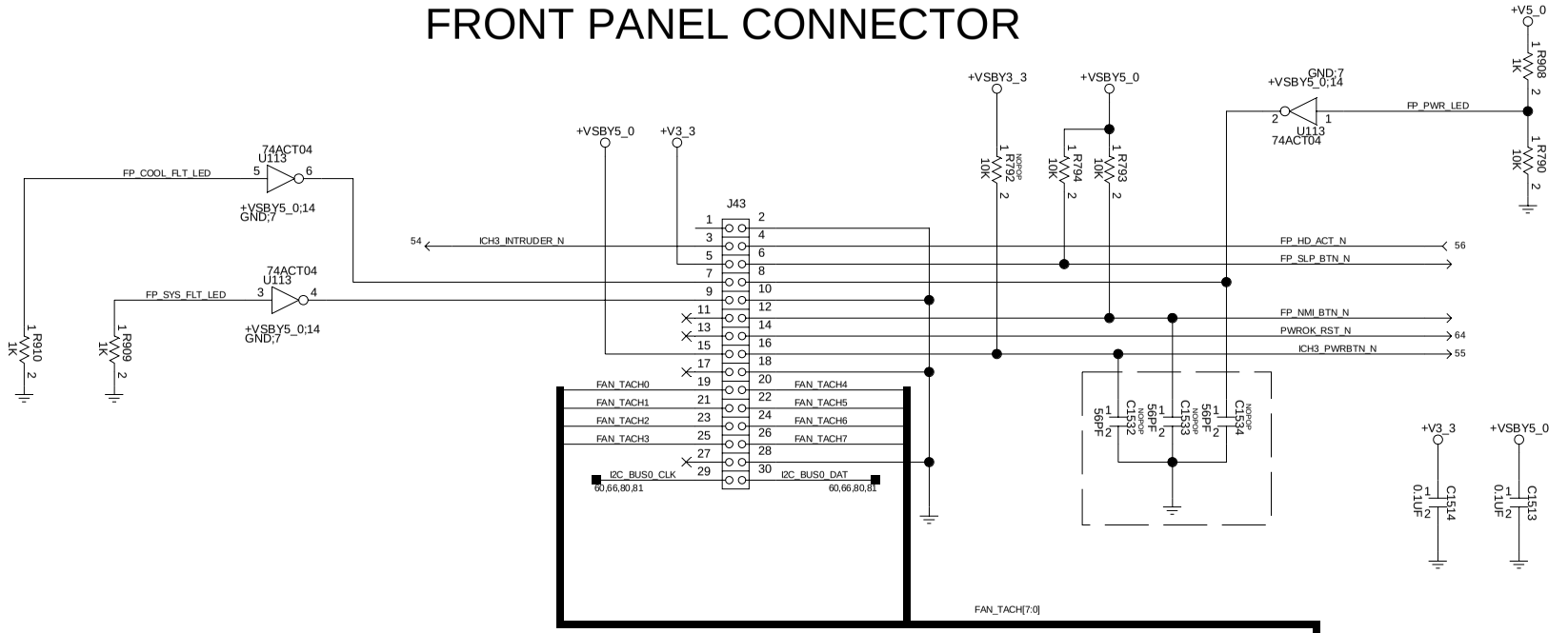
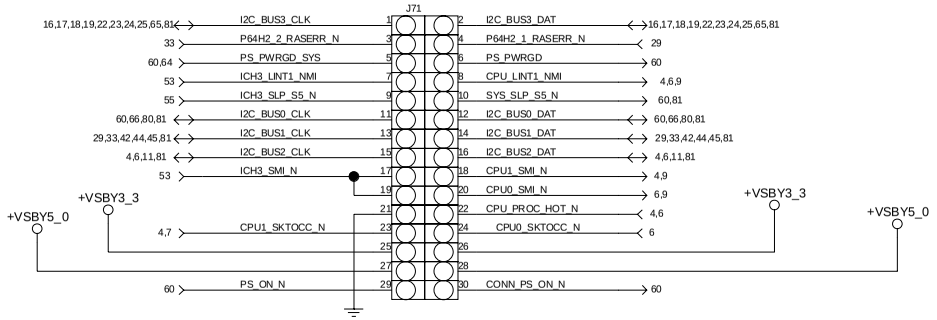
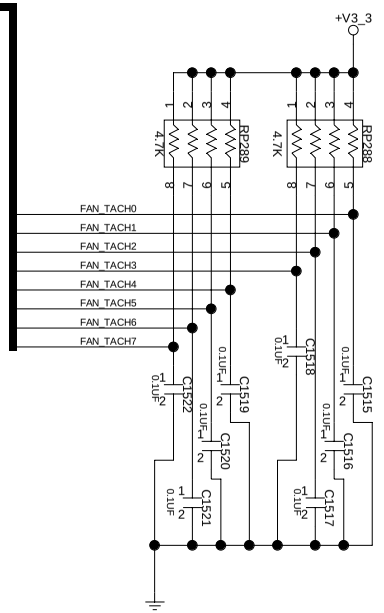
FRONT PANEL CONNECTOR



Install jumpers to short pin pairs
5 and 6, 7 and 8, 9 and 10, 17 and 18,
19 and 20, 29 and 30



BMC Connector
for validation



Pull-ups for fan tach on fan cntl board

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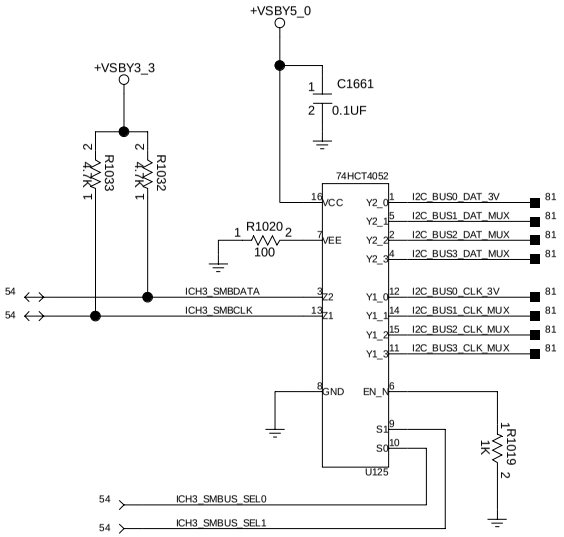
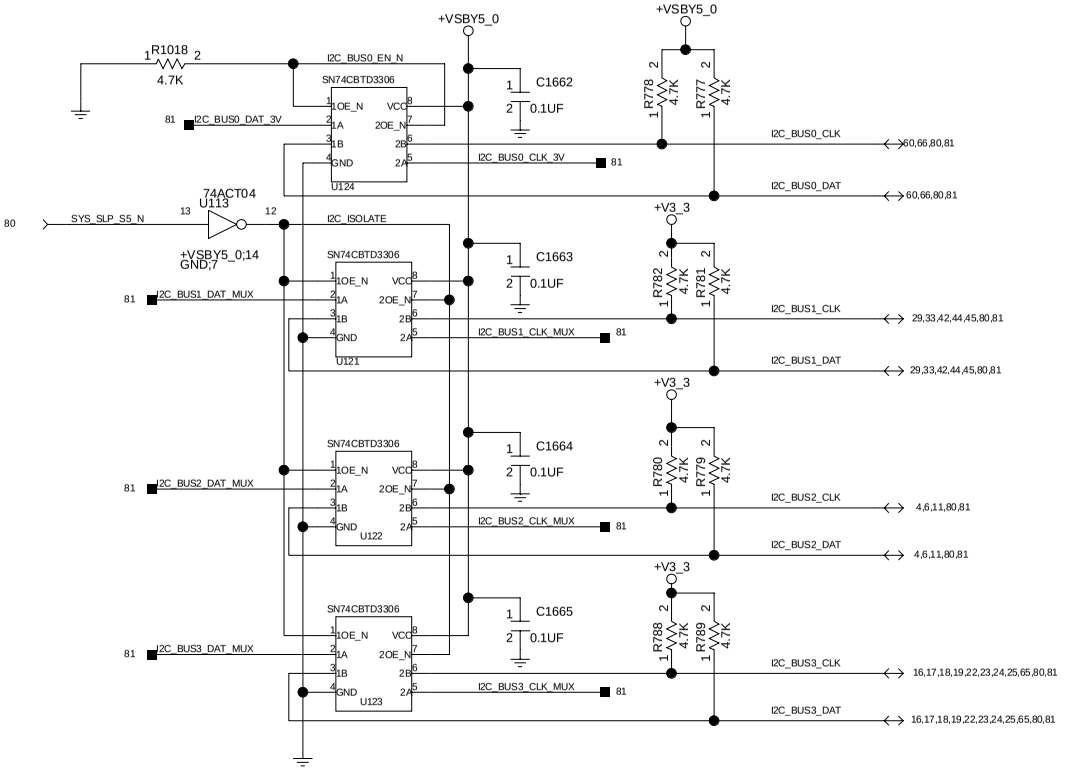
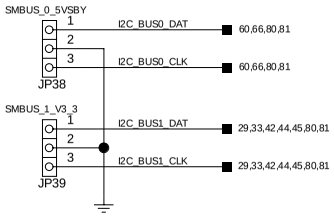
SMBus Mux

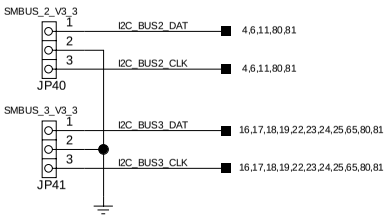


SEL1	SEL0	SMBus Partition
0	0	Bus 0
0	1	Bus 1
1	0	Bus 2
1	1	Bus 3 (default)

SMBus Isolation and Voltage Translation







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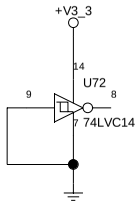
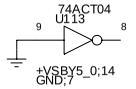
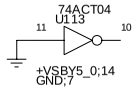
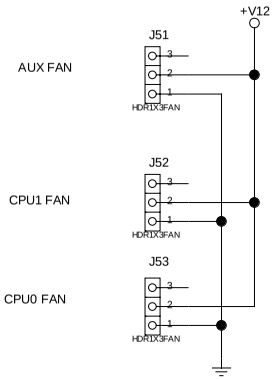
SPARE GATES

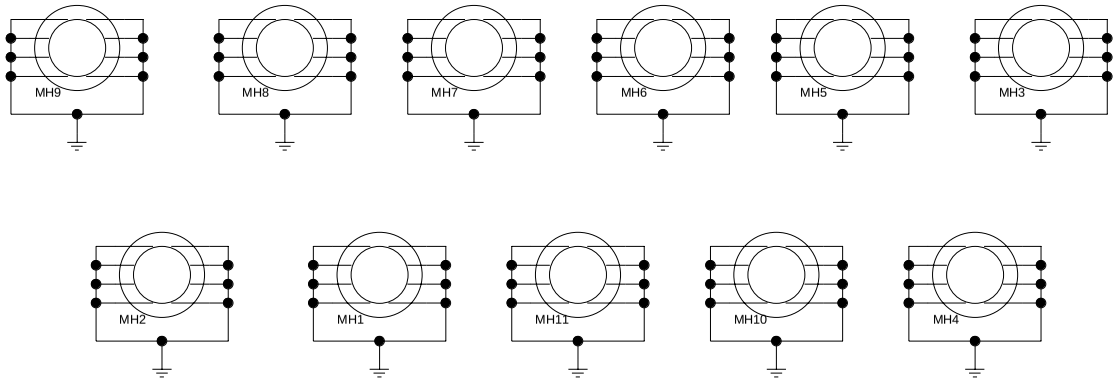




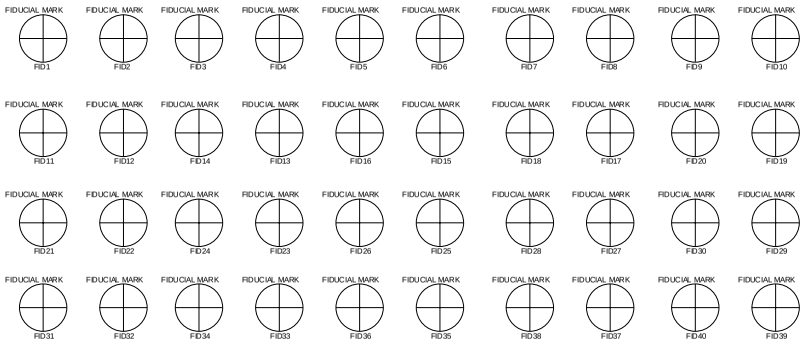




Mounting Holes



Fiducial marks



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I2C BUS 0

Partition Select 00

- Chassis Fan Board EEPROM SMB Address = AAh
- Chassis Fan Board Thermal Sensor SMB Address = 9Ah
- Chassis Fan Board 8-bit I/O (FAN_FAIL) SMB Address = 4Eh
- Chassis Fan Board 8-bit I/O (FAN_PRES) SMB Address = 46h
- Power Supply SMB Address = A6h
- Test Header JP38

+VSBY5_0

I2C BUS 1

Partition Select 01

- P64H2 #1 SMB Address = C2h
- P64H2 #2 SMB Address = C0h
- PCI-X Slot 1 SMB Address Resolution Protocol
- PCI-X Slot 2 SMB Address Resolution Protocol
- PCI-X Slot A SMB Address Resolution Protocol
- PCI-X Slot B SMB Address Resolution Protocol
- PCI-X Slot C SMB Address Resolution Protocol
- PCI-X Slot D SMB Address Resolution Protocol
- Test Header JP39
- BMC Connector J71

+V3_3

I2C BUS 2

Partition Select 10

- Processor 0 IDROM SMB Address = A0h
- Processor 1 IDROM SMB Address = A2h
- Processor 0 Thermal Sensor SMB Address = 30h
- Processor 1 Thermal Sensor SMB Address = 32h
- Plumas MCH SMB Address = 60h
- Test Header JP40
- BMC Connector J71

+V3_3

I2C BUS 3

Partition Select 11 (Default)

- DIMM A-0 SMB Address = A0h
- DIMM A-1 SMB Address = A2h
- DIMM A-2 SMB Address = A4h
- DIMM A-3 SMB Address = A6h
- DIMM B-0 SMB Address = A8h
- DIMM B-1 SMB Address = AAh
- DIMM B-2 SMB Address = ACh
- DIMM B-3 SMB Address = AEh
- CK-408B SMB Address = D2h
- Test Header JP41
- BMC Connector J71

+V3_3

MUX

ICH3-S

SMB Slave Address = 88h

SMBDATA — ICH3_SMBDATA

SMBCLK — ICH3_SMBCLK

GPIO27 — ICH3_SMBUS_SEL0

GPIO28 — ICH3_SMBUS_SEL1

NOTE:
SMBus Addresses expressed as 8-bit hex numbers assume "0" as LSB.
This is actually the Read/Write bit, and may take on either value,
depending on the nature of the transaction.

SMBUS PARTITION MAP

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